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OPERATION AND MAINTENANCE MANUAL
FOR THE
PRO88 FREQUENCY SYNTHESIZER

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OPERATION AND MAINTENANCE MANUAL

FOR THE

PRO88 FREQUENCY SYNTHESIZER

FOR USE IN

TDRSS TRANSPONDER TEST SET

SYNTHESIZER SUBSYSTEM

Issue No. 1, November 1980

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PREFACE TO THE TDRSS

TEST SET SYNTHESIZER EDITION

The PR088 has been modified for the TDRSS Test Set Synthesizer application. In particular, all Multibus interface circuitry has been deleted. This change is reflected in the component layout photo, the schematics, the parts list, and the configuration sheets. The Manual does present discussions of the Multibus interface and programming considerations which are not relevant to the TDRSS Test Set Synthesizer application.

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1. GENERAL DESCRIPTION

The discussion of this section presents a general description of the PR088 Synthesizer. This section also contains a performance specification for the PR088 Synthesizer.

1.1 Synthesizer Characteristics

The PR088 Frequency Synthesizer covers the range from 10 MHz to 200 MHz, with a minimum tuning range of 20% of the selected center frequency. It is universal in nature with the specific operating frequencies available to the user determined by computer programmable frequency selection, on card selectable division ratios and the external frequency input.

A block diagram of the synthesizer is shown in Figure 1-1. This card contains three major synthesizer subsystems. First, a reference phase locked loop is included which either generates a 10 MHz reference from a card mounted crystal oscillator, or it can lock the crystal oscillator to an external 5 or 10 MHz applied input. Next, the card includes a variable modulus synthesizer loop implemented with a CMOS synthesizer chip. Finally, a single side band offset mixer loop is included.

This single-card unit conforms mechanically and electronically to MULTIBUS* standards and is compatible with any other Multibus compatible equip-

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*MULTIBUS is a registered trademark of Intel Corp.

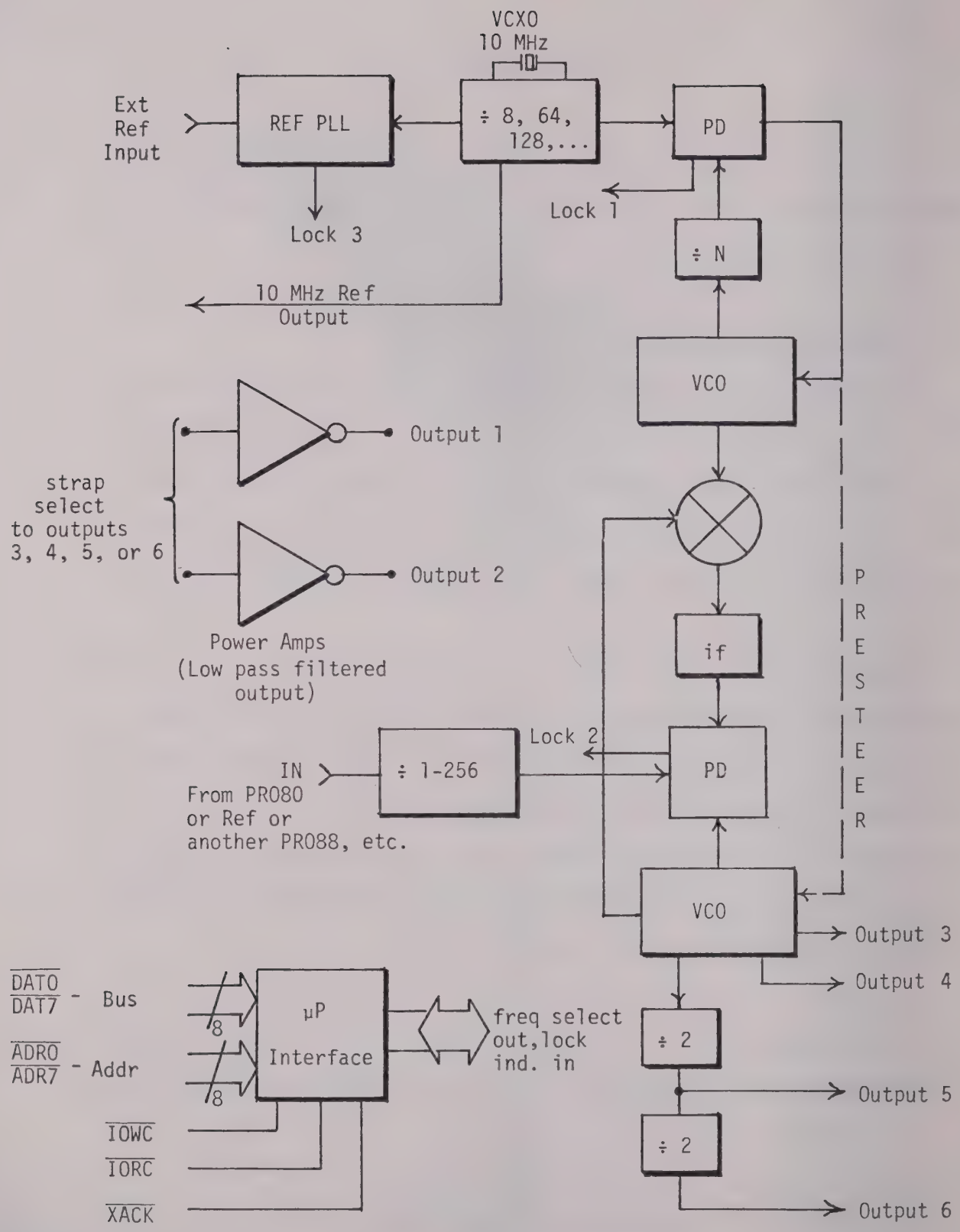

Figure 1-1. SIMPLIFIED BLOCK DIAGRAM

ment. The synthesizer is controlled by transmitting frequency command data from a host microcomputer to the synthesizer through the standard Multibus interface.

1.2 PR088 Synthesizer Specifications

Frequency Range:	10-200 MHz
Tuning Range:	20% of center frequency min.
Step Size:	1.6 MHz, 156.25 kHz, 78.125 kHz, 39.0625 kHz, 15.625 kHz, 10 kHz, and others
Power Output:	+10 dBm sinewave, alternates available, refer to outputs below and block diagram
Waveform:	sinewave, square wave, strap selectable
Harmonics:	-40 dBc (low pass filtered outputs)
Non-Harmonic Spurious Outputs:	-60 dBc
Phase Noise:	60 dB below 1 radian measured in a band from 1 Hz to 30 kHz from carrier, when operated at 100 MHz center frequency and 1.6 MHz step size SSB Phase Noise Density: -110 dBc/Hz @ 10 kHz off carrier, same conditions as phase noise
Frequency Programming:	MULTIBUS compatible - 8080 μP code drivers supplied in commented source code.
Internal Reference Frequency Stability:	100 ppm. Unit may be phase-locked to an external reference at 10 MHz or 5 MHz

Outputs (Refer to Figure 1, levels into 50Ω):	1. High level amplifier, +10 dBm, low pass filtered 2. High level amplifier, +10 dBm, low pass filtered 3. Synthesizer Output, 0 dBm 4. Synthesizer Output, 0 dBm 5. ÷ 2 Synthesizer Output, 0 dBm 6. ÷ 4 Synthesizer Output, 0 dBm High level amplifer inputs may be strap connected to outputs 3, 4, 5, or 6, as desired 7. Reference Output, 10 MHz, LS TTL 8. Lock detector outputs: via Multibus
Inputs:	1. Mixer: Accepts PRO8Ø or PRO88 signals, strap selectable on card division ratios of 1 to 256 are available, prior to mixing 2. Reference: 10 MHz and subharmonics. Other frequencies available, consult factory 3. Frequency programming: via Multibus
Power Requirements:	+5v at 400ma (max) +12v at 100ma Supplied via bus connector
Dimensions:	Compatible with SBC/MDS/BLC card format, i.e., system consists of a single printed circuit card 12" x 6.75" O.D. pin-for-pin compatible with Multibus connector*

1.3 Configuration

The universal nature of the PRO88 permits its configuration to be adapted for specific applications. Each PRO88 is provided with a configuration

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*See Multibus definition in Intel "Multibus Interfacing", AP-28, available from Intel.

control number which defines its configuration. Appendix B presents the user configuration parameters.

The user may readily reconfigure the PR088 to meet his changing requirements. However, extreme caution and detailed engineering design and engineering design review efforts should be applied if VCO operating ranges and/or loop parameters are changed from the initial configuration.

A PR088 reconfiguration service is provided by the factory. The user should contact the factory for information regarding this service.

2. THEORY OF OPERATION

This section describes the theory of operation of the PR088 Frequency Synthesizer. An overall description is provided. Next, the major functional elements are described.

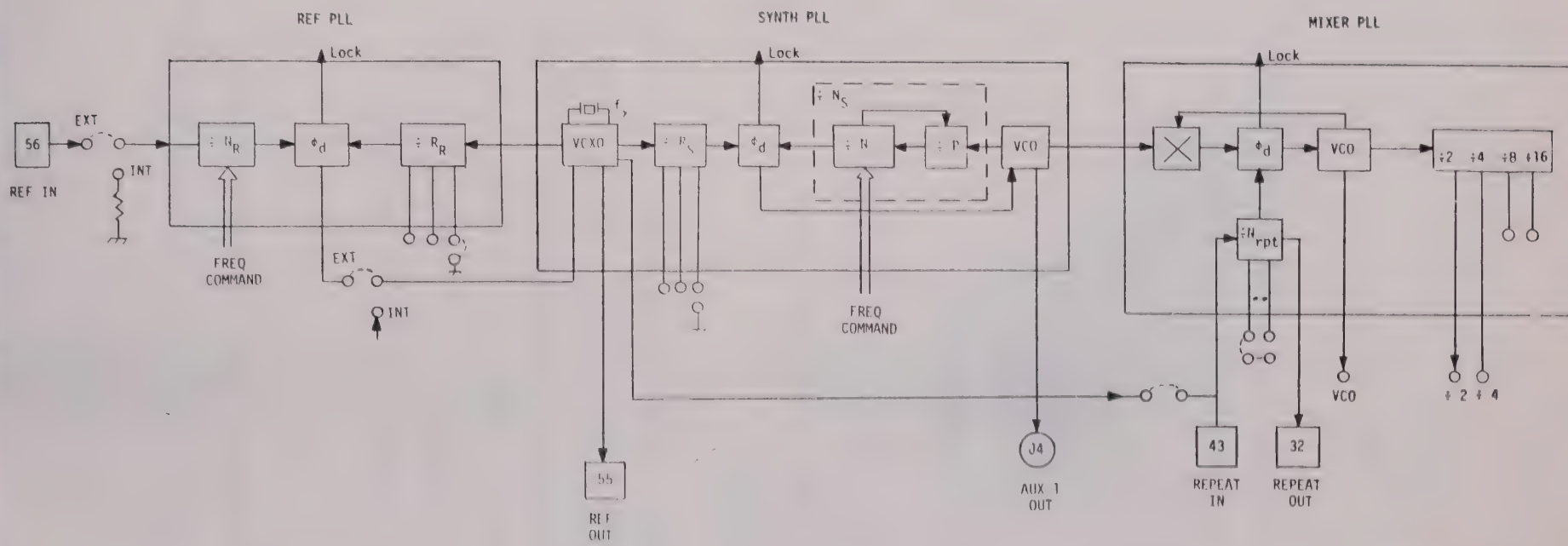
2.1 General Description

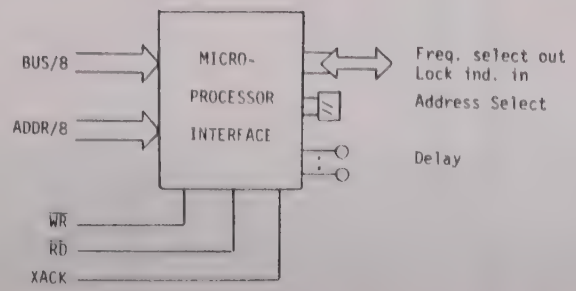
Figure 2-1 presents an overall block diagram of the frequency synthesizer. The unit contains five major subsystems as shown in the figure.

The reference PLL provides the interface between the synth PLL and an external standard. The synthesizer can be strapped to operate on its own internal reference, if desired.

The synth PLL is a single loop digital synthesizer. It provides an output over a selected frequency band in the 10 to 200 MHz frequency region. Its output frequency is determined by a programmable divider, N_s, which is set via the Multibus interface. A reference divider, R_s, is set via straps on the PR088 board. The output frequency, f_o, is related to the reference frequency f_x by $f_o = f_x N_s / R_s$. The resolution of this synthesizer is $\Delta f_o = f_x / R_s$.

The mixer PLL provides a phase locked mixer offset capability for the synth loop PLL. Similar to the synth loop, it contains a VCO operating





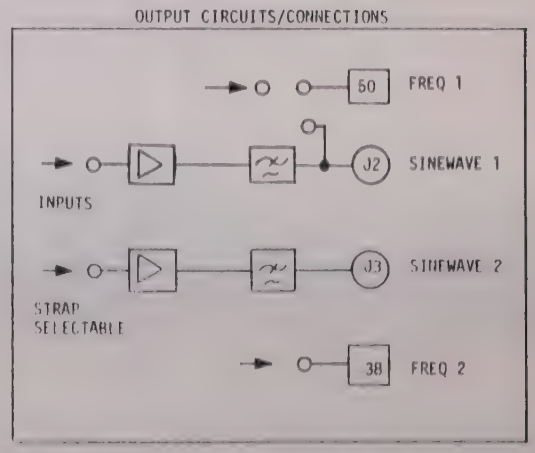


Figure 2-1. PROBB BLOCK DIAGRAM

over a selected portion of the 10 to 200 Mhz frequency range. It provides buffered VCO, VCO ÷ 2, and VCO ÷ 4 outputs, if desired.

The synthesizer output signal from the mixer PLL can be provided as an ECL logic level or as buffered, low pass filtered, sine wave signal with levels of up to +10 dBm. The output configuration is strap selectable and set up per the user requirement.

The Multibus interface circuitry provides a means for recognizing data on the bus which is addressed to a particular PROBB synthesizer card. This data controls the programmable divider of the reference and synth phase locked loops (PLL).

2.2 Frequency Relationships

This section summarizes the frequency relationships of the synthesizer functional elements. Additional information is provided in the detailed description of the functional elements.

2.2.1 Reference PLL

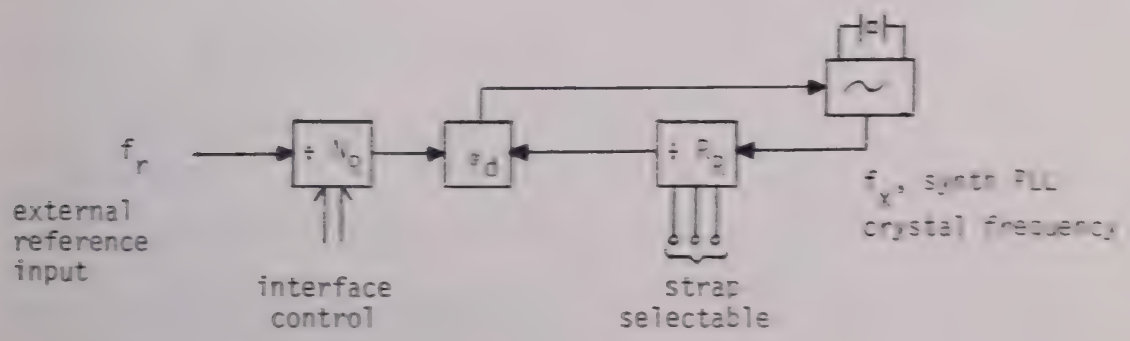


Figure 2-2. SIMPLIFIED REFERENCE PLL

$$f_r = \frac{N_R f_x}{R_R}$$

where N_R = 3 to 1023

R_R = 8, 64, 128, 256, 640, 1000, 1024, 2048

f_r synth = 1-12.8 MHz, chosen for synth PLL step size and f_r compatibility

f_x = synth PLL crystal frequency

Note: f_r/N_r < 1.5 MHz

2.2.2 Synthesizer PLL

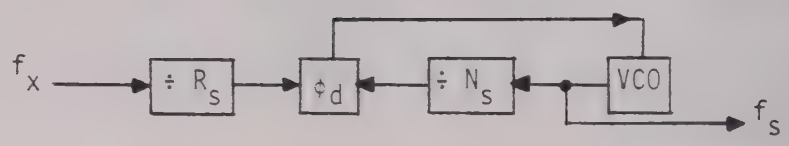


Figure 2-3. SIMPLIFIED SYNTH PLL

$$f_s = \frac{N_s f_x}{R_s}$$

where N_s = 56-8191, for P = 8

R_s = 8, 64, 128, 256, 640, 1000, 1024, 2048

f_s = synth VCO output frequency

Δf_s (step size) $= \frac{f_x}{R}$

Note: f synth VCO < 200 MHz

$\frac{f_x}{R}$ < 1.7 MHz

N_s determined by ÷ P and ÷ N characteristics - see Table 2-1

2.2.3 Mixer PLL

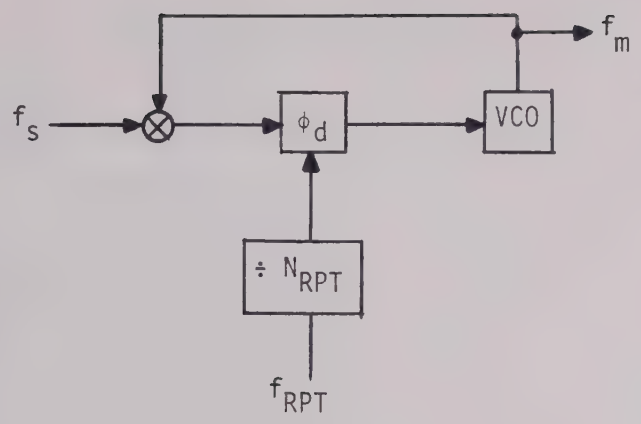


Figure 2-4. SIMPLIFIED MIXER PLL

$$f_m = f_s \pm \frac{f_{RPT}}{N_{RPT}}$$

where:

f_m = mixer VCO output frequency

f_s = synth VCO frequency

f_{RPT} = Repeat input frequency

N_{RPT} = Repeat input divide ratio, 1-256 (strappable)

Note: F_s <200 MHz

f_{RPT} <200 MHz

$\pm$ depends on application, set up for either + or -.

2.2.4 Final Output

In the case where the synth loop feeds the mixer loop:

$$f_{out} = \frac{N_s f_x}{R_s} + \frac{f_{RPT}}{N_{RPT}}$$

2.3 Reference PLL Description

The major elements of the loop are a CMOS synthesizer integrated circuit (U16), passive loop filter, VCXO (part of synth loop CMOS integrated circuit (U17), and lock detector interface, as can be seen in Figure 2-5. U16 is Motorola's part number MC145156 and contains divider/prescaler control logic, reference divider, programmable divider, phase detector and lock detector circuitry. The reader is referred to Motorola's data sheet for the particulars on this device. A summary of the MC145156 characteristics is shown in Table 2-1. For this application, the divider ratios of Section 2.2.1 apply. Note that the programmable divider is controlled via the Multibus interface, while the reference divider ratio is strap selectable.

PLL operation is described as follows: The loop error signal is derived from the phase detector of U16 by comparing the divided synth loop frequency with the divided external reference frequency

$$\left(\frac{f_r}{N_R} = \frac{f_x}{R_R} \right)$$

This signal is applied to a passive loop filter and then to a varactor which corrects the crystal oscillator frequency of U17.

The lock detector output from U16 is provided to U12 and Q2. Q2 drives an on card LED, which when illuminated indicates reference PLL unlock.

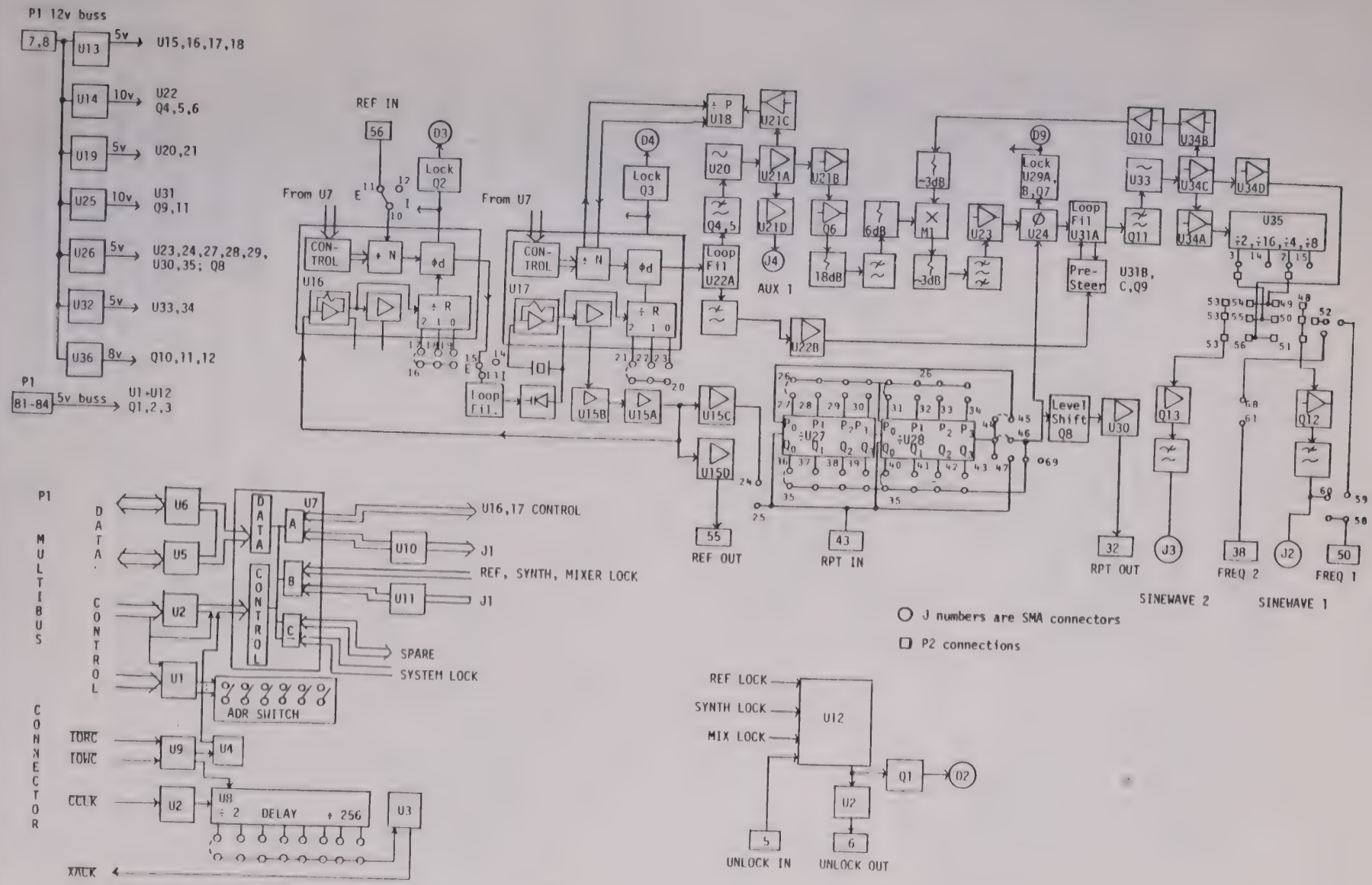
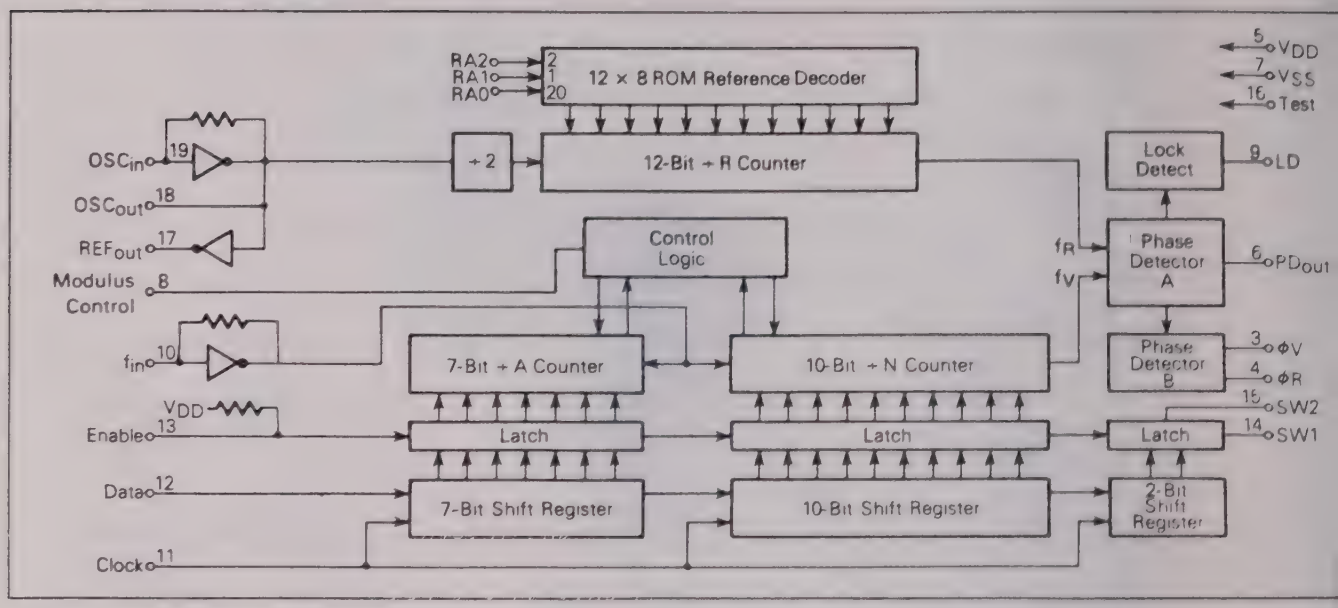


Figure 2-5. PRO88 BLOCK DIAGRAM BY FUNCTIONAL ELEMENT

Table 2-1

U16 AND U17, MC145156 SYNTHESIZER
INTEGRATED CIRCUIT DESCRIPTIVE INFORMATION

1. BLOCK DIAGRAM



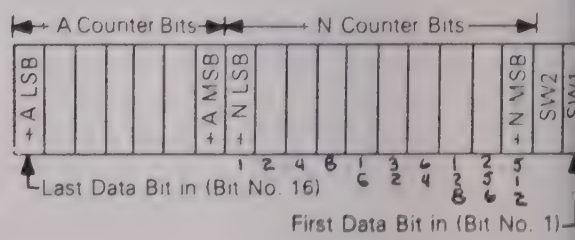
2. REFERENCE DIVIDER

RA0, RA1, RA2 (Pins 20, 1, and 2) — These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	640
1	0	1	1000
1	1	0	1024
1	1	1	2048

3. PROGRAMMABLE DIVIDER

CLOCK, DATA (Pins 11 and 12) — Shift register clock a data input. Each low-to-high transition clocks one bit in the on-chip 19-bit shift register. The data is presented on t DATA input at the time of the positive clock transition. T DATA input provides programming information for t 10-bit ÷ N counter, the 7-bit ÷A counter and the tw switch signals SW1 and SW2. The entry format is follows:



Note: In the reference PLL, A = 0, and $N = N_S$; ref. Figure 2-1.

ENABLE (Pin 13) — When high ("1") transfers contents the shift register into the latches, and to the programmal counter inputs, and the switch outputs SW1 and SW When low ("0") inhibits the above action and thus allo changes to be made in the shift register data without affe ing the counter programming and switch outputs. An c chip pull-up establishes a continuously high level ENABLE when no external signal is applied to Pin 13.

Loop filter parameters have been chosen to optimize loop performance and are tailored to the user requirements. In general, the divider ratios are made as low as compatible with f_r and f_x frequencies in order to keep the phase detector operating frequency high, thereby minimizing the high frequency filtering requirements on the VCXO control line. The loop bandwidth is in the 1 to 2 Hz range, thus assuring a noise free reference signal to the synth PLL.

Specific operating parameters are presented in Appendix B.

Note: When the PR088 is operated from the internal reference source (U17-Y1), implemented by on card connections, this circuit is not functional.

2.4 Synthesizer PLL Description

Figures 2-1 and 2-5 present general and detailed functional synthesizer PLL relationships. The synthesizer loop is comprised of a CMOS synthesizer integrated circuit (U16), an ECL ÷ P prescaler (U18), active loop filter (U22A), active low pass filters (Q4, Q5), VCO (U20), VCO buffer amplifiers (U21) and reference buffer amplifier (U15). Loop operation is described below.

The loop error signal is derived by the phase detector of U17 by comparing the divided VCO frequency with the divided crystal frequency, f_x. This signal is applied to an active loop filter and to the VCO control varactor through active low pass filters Q4 and Q5. Another output from the loop

filter is filtered and buffered by U22B and provides a presteer input to the mixer PLL. The VCO output is buffered (U21A) and then applied to three separate buffers (U21B, C, and D). As can be seen from Figure 2-5, U21C drives the ÷ P prescaler (U18) whose output feeds the synthesizer chip and thus closes the loop. U21B provides a VCO output to the mixer PLL. U21D provides a VCO output, to SMA connector J4.

U17 provides a loop lock signal which is provided to U12 and to Q3 which drives the on card unlock indicator (D4). In addition, this IC (U17) provides a buffered reference oscillator output which feeds the buffer amplifier within U15. Thus, the U17 crystal reference signal is fed to the reference PLL, the outside world (via P2-55) and may be connected to the repeat input if so desired.

The programmable and reference divider characteristics are summarized in Table 2-1. The reader is referred to Motorola's MC145156 data sheet for additional descriptive information for U17.

Loop parameters have been optimized to conform with the user requirement. Appendix B presents the specific parameters for the user configuration.

Note, that in this application the MC145156 is used with, and controls, prescaler (U18).

The modulus control level provided by U17, pin 8 will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N-A additional counts, since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value ($N_s = N \cdot P + A$ where P and P + 1 represent the dual modulus prescaler divide values respectively for low and high modulus control levels; N the number programmed into the ÷ N counter and A the number programmed into the ÷ A counter.

<u>Synth Loop Programmable Divider Range</u> The system total divide value (N_s) will be dictated by the application, i.e.,

$$N_s = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \cdot P + A$$

N is the number programmed into the ÷ N counter; A is the number programmed into the ÷ A counter. P and P + 1 are the two selectable divide ratios available in the two modulus prescalers. To have a range of N_s values in sequence, the ÷ A counter is programmed from zero through P - 1 for a particular value N in the divide N counter. N is then incremented to N + 1 and the ÷ A is se-

quenced from zero through P - 1 again.

There are minimum and maximum values that can be achieved for N_s. These values are a function of P and the size of the ÷ N and ÷ A counters. The constraint N > A always applies. If $A_{max} = P - 1$, then $N_{min} > P - 1$. Then $N_{s_{min}} = (P - 1) P + A$ or $(P - 1) P$ since A is free to assume the value of zero.

$$N_{s_{max}} = N_{max} \cdot P + A_{max}$$

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

When the PR088 is operated using Y1 as the primary reference frequency source, the reference frequency may be trimmed by R3 (refer to Section 5, Schematics). This adjustment applies a voltage to the VCXO tuning varactor which will trim the frequency of operation of the crystal.

2.5 Mixer PLL Description

The PR088 single sideband offset mixer loop is implemented via a double-balanced mixer (M1), high speed ECL phase detector (U24), VCO (U33) and associated circuits as illustrated by Figures 2-1 and 2-5.

The loop operates as follows: The loop error signal is derived by phase detector U24. The inputs to the phase detector are the divided repeat input signal and the output of the double-balanced mixer, M1. The mixer output is determined by the beat between the mixer loop VCO, U33 and the buffered (Q6) low pass filtered output from the synthesizer loop VCO buffer, U21B. The phase detector error signal is applied to an active loop filter (U31A) and then further filtered by an active filter implemented with Q11. The output of this filter is then applied to a varactor which determines the VCO, U33, operating frequency. During initial loop lock-up a VCO presteer signal from the synthesizer PLL is applied via U31B, C and Q9 to the VCO control varactor to aid VCO lock up and to ensure that the VCO is on the correct side of the synthesizer VCO frequency. Buffered VCO, VCO divided by two and VCO divided by 4 outputs are available for use as desired. In addition, the divided repeat input signal is provided at P2-32.

Appendix B presents the user configuration for this functional element.

2.6 Output Circuits

A variety of output configurations are available to the user as can be seen in Figure 2-5. These are strap selectable and have been configured to meet user requirements. The applicable configuration is presented in Appendix B.

Two buffer amplifiers (Q12 and Q13) with integral low pass filters may

be used to amplify the synthesizer VCO, mixer VCO, mixer VCO divided by 2, and/or mixer VCO divided by 4 signals to levels of +10 dBm, as desired.

In addition, these output signals may be provided to either the card edge connector (P2) or to SMA jacks (J2, J3).

2.7 Interface Circuits

The lower left portion of Figure 2-5 presents the functional elements associated with the synthesizer bus interface. U1 recognizes the control address as determined by the address switch setting. Switch operation is explained in Section 3.3. Once the address has been recognized, the logic of U9 and U4 enable $\overline{IORC}$ and $\overline{IOWC}$ signals and operation of the 8255 (U7),peripheral interface control device may commence. Bi-directional bus data is handled via U5 and U6 under U7 control. In addition, U7 sends frequency control data to synthesizer IC's U16 and U17. Synthesizer subsystem lock signals and a system $\overline{lock}$ signal (via U12) are sent to the 8255 for use in computer fault detection and analysis. U10 and U11 are user selected peripheral interface devices that are also under U7 control. 8255 usage is discussed in more detail in Sections 2.8, 3.7, and 3.10.

The $\overline{XACK}$ response time may be adjusted by selecting the appropriate output from U8.

2.8 Programming Characteristics

The PR088 Multibus interface is implemented using an 8255 programmable

peripheral interface chip. The host microprocessor must provide a routine which initializes the 8255. After initialization, the host microprocessor must operate a routine which outputs the frequency command data to the 8255 and then to the synthesizer chips. Following the output routine, the host microprocessor may execute a routine which transfers the synthesizer lock status to the host microprocessor. Table 2-2 shows the organization of the ports.

Table 2-2

8255 PORT IDENTIFICATION

PORT	ADDRESS	CONTENT	
A	Synth Address + 0	PAØ	Synth chip data clock
		PA1	Synth chip freq data
		PA2	U16 synth chip enable (N_{REF})
		PA3	U17 synth chip enable (N_{SYNTH})
		PA4,5,6,7	To user chip U10
B	Synth Address + 1	PBØ	Ref lock
		PB1	Synth lock
		PB2	Mixer lock
		PB3	Not Used
		PB4,5,6,7	To user chip U11
C	Synth Address + 2	PCØ	System lock
		PC1-PC7	Not used
Control	Synth Address + 3		Configuration word

During the initialization process, the 8255 control port must be addressed by the host microprocessor and provided with the appropriate configuration word. A sample initialization program and other operating programs are given in Section 3. After initialization the frequency command data must be loaded via port A into synthesizer chips U16 and U17. Once this is accomplished, synthesizer lock status may be determined from ports B or C. The addresses of each of these data and control ports is equal to the synthesizer address, plus a number between 0 and 3. The synthesizer address is selected by means of a DIP switch mounted on the PR088 board. Table 2-3 summarizes the possible synthesizer addresses.

Table 2-3

SYNTHESIZER ADDRESSING

Dip Switch Value/ Synth Address (Hex)	Addresses of 8255 Ports (Hex)			
	PA	PB	PC	Control
0	0	1	2	3
4	4	5	6	7
8	8	9	A	B
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
F4	F4	F5	F6	F7
F8	F8	F9	FA	FB
FC	FC	FD	FE	FF

Note that 64 unique synthesizer addresses are possible. The table assumes that the host microprocessor is an Intel SBC 80/10. In that case, some of the addresses in the range from E0 to EF are used by the SBC 80/10. This makes them unusable by the PR088 board. Note that other host microprocessor systems may be more or less restrictive on the choice of synthesizer addresses.

3. SYSTEM INSTALLATION AND INTERFACING

This section defines a step-by-step procedure for establishing operation of the PR088 Frequency Synthesizer.

3.1 Unpacking

Carefully inspect the PR088 board for any damage which may have been incurred during shipping. If the board appears to be damaged, return it immediately to Proteon Associates. Do not attempt to repair the board unless given authorization in writing from Proteon Associates. Any unauthorized repair may void the warranty. Please obtain a Return Authorization from the factory before returning the unit.

Proteon makes extensive use of IC sockets on the board. This will facilitate repair and maintenance of the system. Check to see that all integrated circuits are firmly inserted in their sockets.

3.2 PR088 Configuration

The user configuration is defined in Appendix B. Review this information thoroughly prior to equipment usage.

3.3 Address Designation

Review the characteristics of the host microcomputer and its associated add-on memory, etc. Determine which Bus addresses are available to the PR088 synthesizer. The selected address is implemented on the PR088 card using the 8-position DIP switch, oriented as shown in Figure 3-1, the most significant

hexidecimal digit of the address is determined by the 4 rocker switches on the right.

A logic "one" is obtained by depressing the end of the rocker which is near the numbers. A logic "zero" is obtained by depressing the end of the rocker which is near the word "open". The PR088 requires four consecutive addresses. As a result, the user can only set the 6 MSB's of the 8 bit PR088 address. Table 2-3 gives the possible addressing switch values.

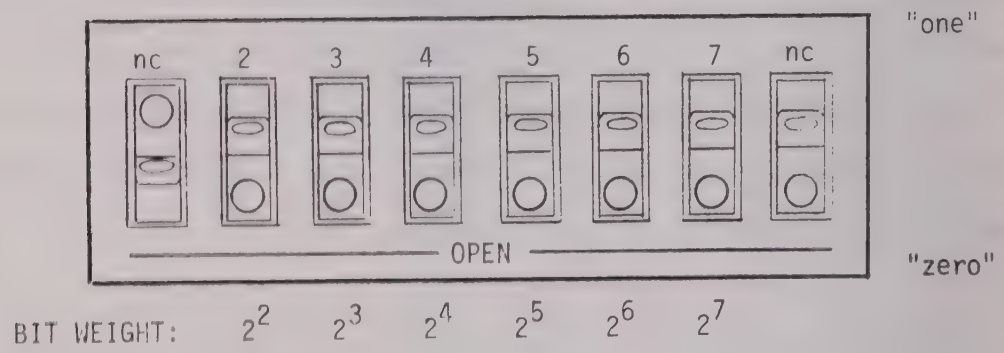


Figure 3-1. ADDRESSING DIP SWITCH

3.4 $\overline{\text{XACK}}$ Delay

The $\overline{\text{XACK}}$ response time may be adjusted by selecting taps on binary divider U8 by strapping terminals as shown in Table 3-7.

3.5 Electrical Requirements

The synthesizer requires DC voltages as shown in Table 3-1.

Table 3-1

ELECTRICAL REQUIREMENTS

DC Voltage	Symbol	Current	Multibus Pin(s) (P1)
+5v	VCC	400ma(max)	3, 4, 5, 6, 81, 82, 83, 84
+12v	VDD	100ma	7, 8
-12v	VAA	--	79, 80
ground	GND	--	1, 2, 11, 12, 75, 76, 85, 86

The data presented in Table 3-1 is in conformance with Multibus standards.

3.6 Electrical Connections

Figure 3-2 shows an outline drawing of the PR088 card which illustrates the locations of the various connectors. Table 3-2 lists sources of compatible connector hardware for the PR088.

Table 3-3 defines the pin assignment of the Multibus connector (P1) used in the PR088. Table 3-4 defines pin assignments of the Auxiliary connector (P2) and Table 3-5 defines pin assignments for the I/O connector (J1). Table 3-6 summarizes SMA connections.

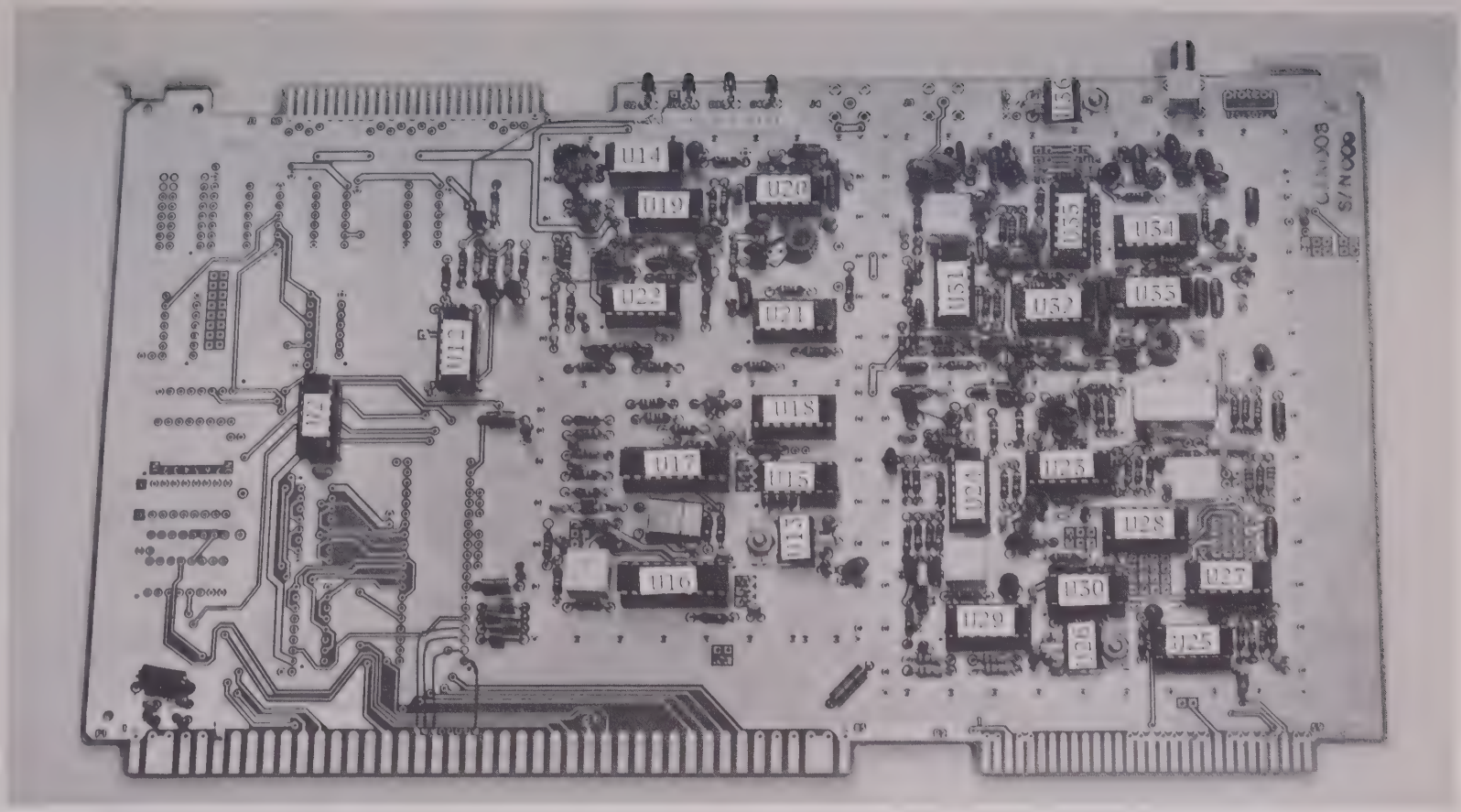


Figure 3-2. PR088 OUTLINE

(TDRSS Test Set Synthesizer)

Table 3-2

PRO88 COMPATIBLE CONNECTOR HARDWARE

Function	No. of Pins	Centers (inches)	Connector Type	Vendor	Vendor Part No.
1. BUS P1	43/86	0.156	Soldered	CDC Micro Plastics Arco Viking	VPB01E43D00A1 MP-0156-43-BW-r AE443WP1 less ears 2VH43/1AV5
2. BUS P1	43/86	0.156	Wirewrap	CDC CDC Viking	VFB01E43D00A1 or VFB01E43A00A1 2VH43/1 and 5
3. AUXILIARY P2	30/60	0.1	Soldered	Viking TI	3VH30/1JN5 H312130
4. AUXILIARY	30/60	0.1	Wirewrap	CDC TI	VPB01B30A00A2 H311130
5. PARALLEL I/O J1	25/50	0.1	Soldered	AMP Viking TI	2-583485-6 3VH25/1JV5 H312125
6. PARALLEL I/O J1	25/50	0.1	Flat Crimp	3M 3M AMP Ansley SAE	3415-0000 w/ears 3415-0001 w/o ears 88038-1 609-5015 SD6750 Series
7. PARALLEL I/O J1	25/50	0.1	Wirewrap	TI Viking CDC ITT Cannon	H311125 3VH25/1JND5 VPB01B25D00A1 EC4A050A1A
8. SYNTH OUT J2, J3, J4	1	N/A	SMA	E.F.Johnson or Amphenol, King, or Sealectro	142-0201-006* 142-0221-006 142-0301-006 142-0321-006 142-0202-006 142-0222-006

(*Part Nos. are for E.F. Johnson parts)

Table 3-3

PIN ASSIGNMENT OF BUS SIGNALS ON MULTIBUS BOARD P1 CONNECTOR

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9	−5V	−5Vdc	10	−5V	−5Vdc
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Pri. In	16	BPRO/	Bus Pri. Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 disable RAM
BUS CONTROLS AND ADDRESS	25		Reserved	26	INH2/	Inhibit 2 disable PROM or ROM
	27	BHEN/	Byte High Enable	28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33	INTA/	Intr Acknowledge	34	AD13/	
INTERRUPTS	35	INT6/	Clk	36	INT7/	Data
	37	INT4/	Ref Enable	38	INT5/	TXL Enable
	39	INT2/	TXU Enable	40	INT3/	RXL Enable
	41	INT0/	Not Used	42	INT1/	RXU Enable
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/	Data	64	DATB/	Data
	65	DAT8/	Bus	66	DAT9/	Bus
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79	−12V	−12Vdc	80	−12V	−12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

All Mnemonics © Intel Corporation 1978

Table 3-4

PIN ASSIGNMENTS FOR AUXILLIARY CONNECTOR P2

COMPONENT SIDE		
Pin	Mnemonic	Description
1	GND	Ground
3	"	"
5	---	Unlock Input
7		
9	GND	Ground
11	No connection	
.	"	
25	"	
27	GND	Ground
.	"	"
41	"	"
43	---	Repeat Input
45	GND	Ground
.	"	"
53	"	"
55	---	Ref. Output
57	GND	Ground
59	"	"

CIRCUIT SIDE		
Pin	Mnemonic	Description
2	GND	Ground
4	"	"
6	---	Unlock Output
8		
10	GND	Ground
12	No connection	
.	"	
26	"	
28	GND	Ground
30	"	"
32	---	Repeat Output
34	GND	Ground
36	"	"
38	---	Freq Output 2
40	GND	Ground
.	"	"
48	"	"
50	---	Freq. Output 1
52	GND	Ground
54	"	"
56	---	Reference Input
58	GND	Ground
60	"	"

Table 3-5

PIN ASSIGNMENT FOR I/O CONNECTOR J1

COMPONENT SIDE			CIRCUIT SIDE		
Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	GND	Ground	2	GND	Ground
3	Spare		4	↑	↑
5	"		6		
7	"		8		
9	"		10		
11	PB4	8255 Port B	12		
13	PB5	Input	14		
15	PB6		16		
17	PB7		18		
19	Spare		20		
21	"		22		
23	"		24		
25	"		26		
27	"		28		
29	"		30		
31	"		32		
33	"		34		
35	PA6	8255 Port A	36		
37	PA7	Output	38		
39	PA5		40		
41	PA4		42		
43	Spare		44		
45	"		46		
47	"		48		
49	"		50	GND	Ground

Note: Spare pins are connected to solder pads and may be used as desired; e.g., 8255 Port C connections PC1 through PC7 could be strapped to these pins.

Synthesizer input and output connections and signals are described in Appendix B.

Table 3-6

SMA CONNECTOR ASSIGNMENTS

Ref. Des.	Description
J2	Sinewave 1 output
J3	Sinewave 2 output
J4	Auxilliary 1 output (synth VCO)

3.7 Control Programming

This section presents the programming requirements for the PR088 Frequency Synthesizer. The discussion begins with a description of the programming operations required to initialize, load and operate the PR088 Frequency Synthesizer. Then, specific programming examples are presented which are designed to interface an SBC 80/10 host microprocessor to the PR088. Programming for other host microprocessor systems can be extrapolated from the examples given below.

Basic operation of the PR088 is achieved with three simple routines. The first is an initialization routine which configures the 8255 on the PR088

board. Specifically, port A must be configured for output, and port B and the lower part of port C must be configured for input. Part of port A and part of port B are free for user use as configured. The upper part of port C is an auxilliary port and may be configured by the user as desired. The allowable 8255 port configuration commands are presented in Table 3-7. Figure 3-3 shows a typical initialization routine.

Table 3-7

8255 PORT CONFIGURATION TABLE

Control Byte	Port A	Port B	Port C (lower)	Port C (upper)
83H	output	input	input	output
8BH	output	input	input	input

Both the PROS8 PLL frequency synthesizer and variable PLL synthesizer are programmed by a clocked, serial input, 19 bit data stream. The 19 data bits are defined in Table 2-1 and are discussed in Section 2.4. The code to download the 19 bit data stream into the PROS8 from a host SBC-80 type processor is presented in Figure 3-4 and its operation is discussed below.

The subroutine "LOAD88" is called with 2 arguments. One argument, the address of the 2 most significant bits (MSBs) of the divide by N value, is passed in the HL register pair. The next 2 higher bytes in memory are loaded

```
PRO88 EQUATES

            PRO88     EQU     G0H       ;PRO88 BASE ADDRESS
            PA        EQU     PRO88     ;PORT A 8255
            PB        EQU     PRO88+1   ;PORT B 8255
            PC        EQU     PRO88+2   ;PORT C 8255
            CTL       EQU     PRO88+3   ;CONTROL PORT 8255
            MODE      EQU     83H       ;PA=OUT, PB=IN, PLL=IN, PCU=OUT


;CODE TO INITIALIZE PRO88's 8255

            MVI       A, MODE           ;8255 MODE BYTE
            OUT       CTL               ;OUTPUT TO 8255 CONTROL PORT


;CODE TO READ PRO88 STATUS PORT B

            IN        A, PB             ;READ STATUS PORT B
```

Figure 3-3. 8255 INITIALIZATION

with the 8 remaining bits of "N" and the 7 bits representing the divide by A value. The 3 bytes of memory containing the divide by A and divide by N values are organized such that the first data bit to be output is in the LSB of the byte. The second argument is an enable bit (high to enable) which is passed in the D register. This argument allows the user to select the desired PLL synthesizer.

The port bits used by the routine to load the PRO88 are defined as follows. Port bit PA2 is the reference PLL enable, while port bit PA3 is used

to enable the variable PLL. Both synthesizer loops share the same data line (PA1) and the same clock line (PAØ).

The routine begins by first outputting SW1 and SW2. These 2 bits are set to zero and then loaded into the C register. The subroutine "BITOUT" then loads register A with the data bits in register C, rotates the value in register A such that the next bit to be output is in the 2^1 bit position, and then stores this value in the C register. All the bits in register A, save the next bit to be output, are then set to zero and the result is output to port A. Port bit PAØ is then set high, clocking in the data bit already on PA1. Control is then returned to "LOAD88". The remaining bits are output in much the same manner.

After the 19 bit data stream has been downloaded into the PRO88, the enable line of the desired synthesizer loop is pulsed high.

PRO88 status information can be read from ports B and C lower. Refer to Table 2-2 for PRO88 port assignments. When using an SBC 80 type computer, an IN <PORT> instruction will allow the user to input data from the specified port to register A. Figure 3-3 shows how port B can be read.

Figure 3-4. SUBROUTINE "LOAD88" AND SUBROUTINE "BITOUT"

```
;EQUATES:
    PA EQU 60 H                         ;BASE ADDRESS OF PRO88
    CL EQU 1                            ;CLOCK BIT
;
;FUNCTION LOAD88
;INPUTS:HL - ADDRESS OF 2 MSB'S OF "N"
;            (HL) = 2 MSB'S OF "N"
;            (HL+1) = 8 LSB'S OF "N"
;            (HL+2) = 7 BITS OF "A"
;            THE THREE BYTES OF MEMORY DEFINED
;            ABOVE ARE ORGANIZED SUCH THAT THE
;            FIRST BIT TO BE OUTPUT IS IN
;            THE LSB OF THE BYTE
;       B  - SYNTHESIZER ENABLE
;            D = 4, REFERENCE PLL ENABLE
;            D = 8, VARIABLE PLL ENABLE
;OUTPUTS: 19 BIT DATA STREAM TO PRO88 PORT
;            ADDRESS "PA"
;CALLS: BITOUT
;DESTROYS: A,B,C,H,L, F/F'S
;DESCRIPTION: THIS CODE ALLOWS THE USER TO
;            PROGRAM A PRO88 FROM AN
;            SBC/80 TYPE PROCESSOR. THE
;            ROUTINE GENERATES A 19 BIT,
;            SERIAL, CLOCKED DATA STREAM FROM
;            THE USER SUPPLIED "DIVIDE BY N"
;            AND "DIVIDE BY A" VALUES
;
;OUTPUT SW1, SW2
LOAD88:     MVI C,0                     ;SW1, SW2 = 0
            MVI B,2                     ;# BITS TO OUTPUT
LD200:      CALL BITOUT                 ;OUTPUT NEXT BIT IN BIT DATA STREAM
            DCR B                       ;LOOP UNTIL..
            JNZ LD200                   ;..BITS OUTPUT
;OUTPUT 2 MSB'S OF "N"
            MOV C,M                     ;GET 2 MSB'S OF "N"
            MVI B,2                     ;# BITS TO BE OUTPUT
LD300:      CALL BITOUT                 ;OUTPUT NEXT BIT IN DATA STREAM
            DCR B                       ;LOOP UNTIL..
            JNZ LD300                   ;..BITS OUTPUT
;OUTPUT REMAINING 8 LSB'S OF "N"
            INX H                       ;ADDRESS 8 LSB'S OF "N"
            MOV C,M                     ;GET 8 LSB'S OF "N"
            MVI B,8                     ;# BITS TO BE OUTPUT
LD400:      CALL BITOUT                 ;OUTPUT NEXT BIT IN DATA STREAM
            DCR B                       ;LOOP UNTIL..
            JNZ LD400                   ;..BITS OUTPUT
;OUTPUT 7 BITS OF "A"
            INX H                       ;ADDRESS OF 7 BITS OF "A"
            MOV C,M                     ;GET 7 BITS OF "A"
            MVI B,7                     ;# BITS TO BE OUTPUT
LD500:      CALL BITOUT                 ;OUTPUT NEXT BIT
            DCR B                       :LOOP UNTIL..
            JNZ LD500                   ;..BITS OUTPUT
```

Figure 3-4, cont'd.

```
;SEND ENABLE PULSE
             XRA D                    ;SET ENABLE BIT
             OUT PA                   ;ENABLE DESIRE SYNTH LOOP
             XRA D                    ;CLEAR ENABLE BIT
             OUT PA                   ;DISABLE SYNTH LOOP
             RET
;FUNCTION    BITOUT
;INPUTS:     C
;OUTPUTS:    NEXT BIT IN 19 BIT DATA STREAM
;CALLS       NOTHING
;DESTROYS:   A,C,PORT PA
;DESCRIPTION:THIS CODE POSITIONS AND THEN OUTPUTS THE NEXT
             BIT IN THE 19 BIT DATA STREAM
;
BITOUT:      MOV A,C                  ;GET BITS TO OUTPUT
             RLC                      ;NEXT BIT OUT IN 2' BIT POSITION
             MOV C,A                  ;RESTORE
             ANI 2                    ;MASK OUT ALL BUT NEXT BIT OUT
             OUT PA                   ;OUTPUT TO PRO88
             XRI CL                   ;CLOCK BIT HIGH
             OUT PA                   ;CLOCK IN DATA BIT
             RET
```

4. MAINTENANCE

This section contains maintenance and parts information and procedures used to maintain, align, test and troubleshoot the PR088 Frequency Synthesizer. The maintenance information is divided into preventive maintenance and corrective maintenance. Preventive maintenance provides basic techniques to assist maintenance personnel in scheduling inspections, cleaning, and minor repairs and adjustments. Corrective maintenance provides maintenance personnel with minimum performance standards, test and alignment procedures and troubleshooting information for the frequency synthesizer. Parts information is provided for repair and/or replacement of defective components in the synthesizer. Test equipment required for preventive and corrective maintenance is listed in Table 4-1. Equipment having characteristics equivalent to those listed in the table can be substituted for the equipment listed in the table. To minimize error factors, only calibrated test equipment should be used.

4.1 Factory Service

The PR088 synthesizer is provided with a 180-day warranty. If the unit fails during the initial 180-day period, the unit should be returned to the factory for repair or replacement.

NOTE

Obtain a Return Authorization from the factory before attempting to return any materials to Proteon.

Table 4-1

TEST EQUIPMENT REQUIRED

ITEM	MODEL	QTY.
Spectrum Analyzer	H-P 141T/8552B/8553B/8554L/8555A	1
Electronic Counter	H-P 5360A	1
Digital Voltmeter	H-P 3440A/3445A	1
Signal Generator	H-P 608F, D	1
Power Meter	H-P 431B	1
Oscilloscope	Tektronix 465, 475, or 485	1
Termination, Feedthrough	H-P 11048B	1
Attenuator, 20 dB	Texscan FP-50/1	1

NOTE: Use only listed test equipment or its equivalent.

A card-swapping service is also available for units which need repair beyond the warranty period. Again, a Return Authorization must be obtained from Proteon before any material is shipped to the factory.

Once Return Authorization is received from Proteon, the unit should be carefully packed for reshipment. A solid, sheathed box lined with water-proof material should be used. The unit should be supported and isolated in

the shipping container by a cushioning material to prevent shifting and damage from shock or vibration during transit.

4.2 Preventive Maintenance

The preventive maintenance procedures in this section are intended to aid in obtaining maximum operating life and reliability of the equipment.

4.2.1 Periodic Inspection

The frequency synthesizer unit should be inspected monthly for burned or damaged components, corrosion or fungus accumulation and loose parts. In addition, the reference oscillator on board the card should be calibrated and adjusted monthly following the procedure described below, if the card is operated in the internal reference mode.

4.2.2 Performance Checkout

This section provides data required to carry out the synthesizer performance checkout.

Performance checkout is accomplished with the aid of a host microprocessor which is programmed to provide single output frequencies such as described in Section 3.9. The performance checkout setup is shown in Figure 4-1.

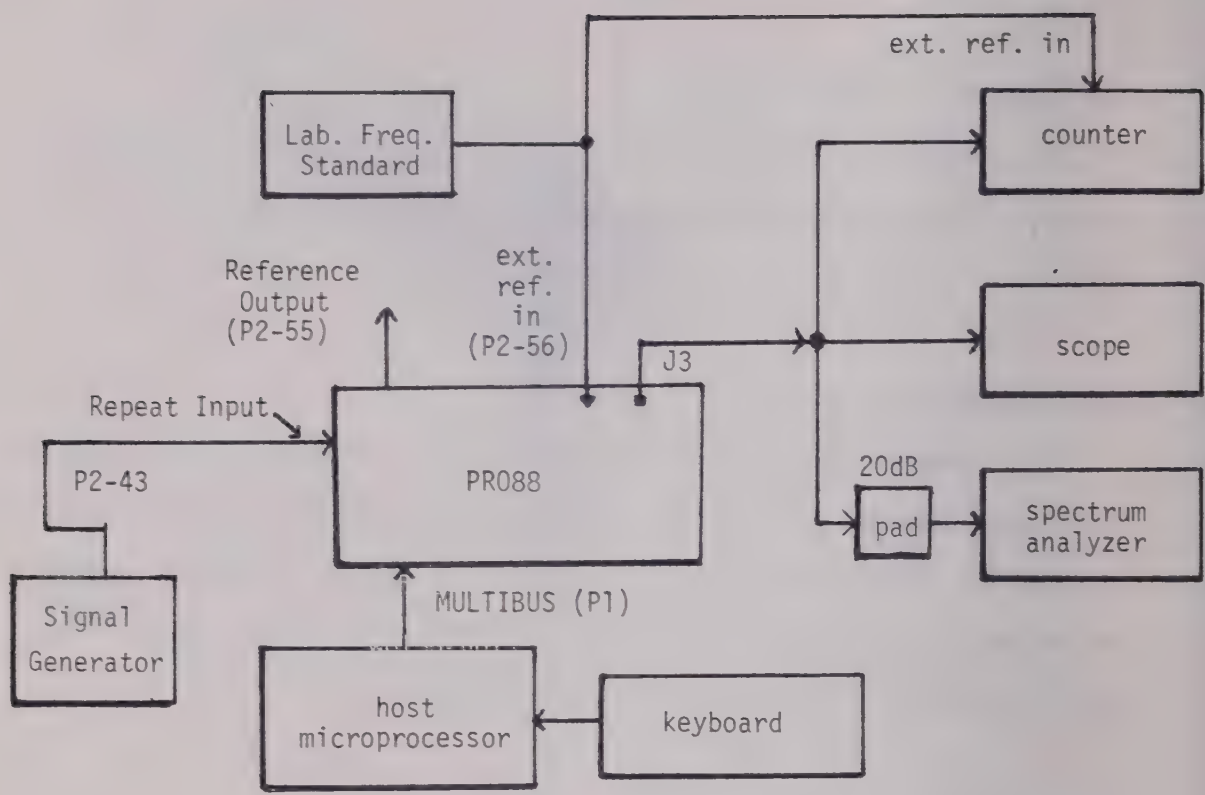


Figure 4-1. PERFORMANCE CHECKOUT - General Set-Up and Connection

Command the PR088 over the frequency ranges determined by N_R, N_S, and the Repeat Input frequency ranges as specified in Appendix B.

Observe the appropriate output signals and check frequency, harmonic content, spurious output and power output with the frequency counter, spectrum analyzer and power meter, as applicable. These performance parameters should fall within the levels specified in Appendix B.

Check the reference output by counting the signal at P2-55. In the external reference mode of operation, this frequency will be directly related to the external frequency. In the internal reference mode of operation, this frequency should be that specified for Y1. If the frequency is incorrect, refer to the alignment section below.

If the results described in this section are not obtained, corrective maintenance may be required.

4.3 Corrective Maintenance

Corrective maintenance procedures for the synthesizer are described in this section. If the synthesizer is within its warranty period, do not carry out corrective maintenance. Instead, return the unit for factory repair after a Return Authorization is obtained from Proteon. The unit can be repaired on site using the troubleshooting procedure given below.

4.3.1 Troubleshooting Procedure

This subsection presents a troubleshooting procedure which should be employed if the factory repair service is not used. The procedure is presented in Table 4-2. Figure 3-2 shows locations of ICs, test points, and trimmers.

Fault Indicators. The synthesizer system is equipped with built-in test indicators. In particular, each of the synthesizer subsystem PLLs has a $\overline{\text{lock}}$-detector circuit which energizes an LED mounted on the edge of the printed circuit card as shown in Figure 3-2. In addition, all of the $\overline{\text{lock}}$ indicator outputs are combined logically to illuminate a system $\overline{\text{lock}}$ indicator LED. The system $\overline{\text{lock}}$ indicator will be illuminated if any of the synthesizer loops is unlocked.

Thus, the system $\overline{\text{lock}}$ indicator is a primary fault isolation device. Given that this indicator is illuminated, troubleshooting should proceed as follows: Observe the edge mounted LED $\overline{\text{lock}}$ indicators. If one of these is illuminated, then the fault is probably in the circuitry associated with that PLL.

Subsystem PLL Observation. Each of the subsystem PLLs has an output connection. The reference PLL may be observed at P2-55, the synthesizer PLL may be observed at the appropriate SMA connector or P2 connection. The outputs may be monitored using a spectrum analyzer or a wideband oscilloscope.

Table 4-2

TROUBLESHOOTING PROCEDURE

Fault Indication	Test Condition	Action
All lighted	Observe LED $\overline{\text{lock}}$ indicators D2, D3, D4, D9	Normal before U16, U17 command
None lighted	Same	Check +12v, +5v Buss Check on card regulators
All lighted	Same	When strap selected for INT. Check internal ref. osc. Y1 and U17
D2, D4, D9 lighted	Same	Check program information to U17 Check for pin 10 of U17
D2, D3 lighted	Same	Check program information to U16 Strap selector set to EXT but no external ref applied Check +5v on U16 Strap selector set to INT but no ref at pin 9 of U16 Check U15
D9 lighted	Same	Check synth loop and mixer loop output frequencies Check for mixer ref signal at pin 6 of U24

Note, however, that the output of a particular subsystem may appear to be normal on the wideband oscilloscope when, in fact, the associated loop is unlocked. Unlock is best determined by the use of a frequency counter or a spectrum analyzer. The spectrum analyzer can determine unlock when the resolution is set at 300 Hz or less, and is useful in observing the synth and mixer PLLs. Alternatively, lock can be verified by direct observation of the voltage control applied to the loop under investigation.

4.4 Alignment Procedure

To ensure maximum performance, the synthesizer must be aligned after repair or replacement of any components on the unit. These procedures must also be performed if the performance tests cited above are not satisfied.

4.4.1 Reference Oscillator - Frequency Set

The alignment described herein should be conducted with the PR088 configured for internal reference oscillator operation only. Observe the reference oscillator frequency at P2-55 with a frequency counter. Adjust R3 for a frequency equal to that of Y1 within 100 Hz.

Note: When operated in the external reference mode without the reference input signal, the reference oscillator may operate at a frequency somewhat offset from the specified crystal frequency. This is normal. Upon application of the reference frequency the internal reference frequency will be corrected so that it is phase locked to the external frequency or sub-

multiple thereof as determined by the U16 programmable divider. The lock indicator will illuminate with removal of the external reference signal.

4.4.2 Synthesizer Loop Alignment

a. Connect scope and voltmeter to phase error test point at R46-R34 junction. Connect counter to AUX1 output.

b. With the loop operating at its upper frequency limit (refer to Appendix B) and locked, the voltage at the phase error test point should be that specified in Section 8 of Appendix B. If this voltage is not observed, an adjustment of the VCO coil may be required. This is done by spreading (to decrease voltage) or squeezing (to increase voltage) the VCO coil turns.

CAUTION

Verify all other components on the card are functioning properly except for frequency before disturbing the coil. This is a delicate adjustment.

After adjustment, apply Q-dope to the coil.

4.4.3 Mixer Loop Alignment

This section discusses alignment of the VCO and phase detector circuits of the mixer PLL.

a. Remove U24. Jumper U24 pins 12 and 13 to +5 VDC (U24-1&14).

b. Set R102 fully counter-clockwise.

c. Check VCO presteer voltage at U311. Voltage should be that specified in Appendix B. If voltage is incorrect, recheck loop card alignment.

d. Check VCO output. It should be that specified in Appendix B. If it is not, adjust VCO coil turns as described previously for the loop card VCO. Again, this is a sensitive adjustment.

e. Adjust R102 for the voltage, specified in Appendix B, between U31, pins 5 and 10.

f. Remove jumpers. Install U24 and verify proper operation.

4.4.4 Phase Detector Alignment

a. Observe the output at pin 9 of U24 with the oscilloscope. Adjust R63 to produce a 50% square wave at pin 9 of U24.

b. With the loop operating normally, observe the waveforms at pins 3 and 12 of U24. Adjust R71 to minimize the pulse durations, simultaneously.

4.5 PARTS LIST

PARTS LIST

ASSEMBLY NAME: _____

ASSEMBLY NO.: _____

ASSEMBLY DRWG. NO.: _____

JOB NO. _____

pro88™ Microprocessor Compatible Frequency Synthesizer

[ ]used on C/N 001, 003 only

ITEM NO.	DESCRIPTION	REF. DES.	PART NO./DRWG. NO.	MFGR.	REV.	QTY/ UNIT	QTY/ REQ
[ ]	Cap., Monolithic Ceramic, .001 µf @ 50V ± 20%	C42, 75, 76, 88, 94, 99, 112, 115, 116, 119, 123, 124, 127, 131, 132, [143]	CW15C102M	Centralab		16	
	Cap., Monolithic Ceramic, .01 µf @ 50V, ± 20%	C1-12, 15, 16, 18, 20, 22, 24, 26-28, 30, 32-36, 43, 49, 51, 55, 62, 73, 74, 92, 101, 105, 106, 111, 118, 126, 133, 136, 137, 140	CW15C103M	Centralab		45	
	Cap., Dipped Tantalum, .1 µf, @ 35V, ± 20%	C13, 14, 19, 21, 25, 29, 44, 45, 52, 67, 85, 117, 125, 135, 139	TAPS.1M35	ITT		15	
[ ]	Cap., Dipped Tantalum, 1 µf, @ 35V, ± 20%	C23, 38, 46, 50, 56-58, 80, 84, 91, 97, 98, [146, 148]	TAPS1M35	ITT		14	
	Cap., Dipped Tantalum, 10 µf, @ 35V, ± 20%	C31, 37, 47, 53, 59, 70, 89, 95, 138, 141, 142	TAPS10M35	ITT		11	
	Cap., Dipped Silver Mica 100 pf, 50V, ± 5%	C48, 54, 90, 93, 96	DM5FY101J	Arco		5	
[ ]	Cap.,Dipped Silver Mica,150pf	[C147]	DM5FY151J	Arco		1	
	Cap., Monolithic Ceramic (see Config. Sheet)	C41, 61, 63-66, 81, 83, 86, 87, 102, 103, 107, 113	CW15CXXXM	Centralab		14	
	Cap., Dipped Tantalum, (see Config. Sheet)	C39, 40, 82, 100, 104	TAPSXXM35	ITT		5	
[ ]	Cap.,Monolithic NPO, 150pf	[C144,145]	CW15C151K	Monolithic		2	

24 crescent street waltham, mass. 02154 proteon associates, inc.	FSCM NO. 9F914	DRAWN / CHECKED / ISSUED	DATE	USED ON:	DWG. NO. 175-007 REV. Ø
					3-16-81 SHEET 1 of 8

PARTS LIST

ASSEMBLY NAME: _____

ASSEMBLY NO.: _____

ASSEMBLY DRWG. NO.: _____

JOB NO. _____

pro88™ Microprocessor Compatible Frequency Synthesizer

ITEM NO.	DESCRIPTION	REF. DES.	PART NO./DRWG. NO.	MFGR.	REV.	QTY/ UNIT	QTY/ REQ
	Cap., Dipped Silver Mica (see Config. Sheet)	C17, 60, 68, 69, 71, 72, 77-79, 82, 108-110, 120-122, 128-130	DMXX	Arco		19	
	Diode, Signal	D11, 12	1N914	Motorola		2	
	Diode, Hot Carrier	D6-8	MBD101	Motorola		3	
	Diode, Light Emitting	D2-4, 9	5082-4484	H/P		4	
	Diode, Varactor, (see Config. Sheet)	D1, 5, 10	MV/BB	Motorola		3	
	RF Choke	E2	VK200 10/3B	Ferroxcube		1	
	RF Choke	E3-6	10-107	Proteon		4	
	RF Choke	E1, 7-21, 23, 24, 26	10-207	Proteon		18	
	RF Choke	E25	10-307	Proteon		1	
	Inductor (see Config. Sheet)	L1-14	1000-XXX	Proteon		14	
	Transformer, Signal (see Config. Sheet)	T1-4		Proteon		4	

PARTS LIST

ASSEMBLY NAME: _____

ASSEMBLY NO.: _____

ASSEMBLY DRWG. NO.: _____

JOB NO. _____

pro88™ Microprocessor Compatible Frequency Synthesizer

ITEM NO.	DESCRIPTION	REF. DES.	PART NO./DRWG. NO.	MFGR.	REV.	QTY/ UNIT	QTY/ REQ
	Transistor, NPN	Q1	2N3904	National		1	
	Transistor, PNP	Q2,3,9	2N3906	National		1	
	Transistor, NPN	Q4, 5, 11	MPS6571	Motorola		3	
	Transistor, NPN	Q6, 10, 12, 13	2N3563	Fairchild		4	
	Transistor, PNP	Q7, 8	2N3640	Fairchild		2	
	Resistor, Carbon Film, 3.3Ω, ¼W, 5%	R14, 31, 86, 110	SBB0207-3.3Ω	Beyschlag		4	
	Resistor, Carbon Film, 8.2Ω, ¼W, 5%	R96, 98	SBB0207-8.2Ω	Beyschlag		2	
	Resistor, Carbon Film, 10Ω, ¼W, 5%	R60, 62	SBB0207-10Ω	Beyschlag		2	
	Resistor, Carbon Film, 12Ω, ¼W, 5%	R54	SBB0207-12Ω	Beyschlag		1	
	Resistor, Carbon Film, 15Ω, ¼W, 5%	R56, 58	SBB0207-15Ω	Beyschlag		2	
	Resistor, Carbon Film, 22Ω, ¼W, 5%	R48, 65	SBB0207-22Ω	Beyschlag		2	
	Resistor, Carbon Film, 39Ω, ¼W, 5%	R53, 55	SBB0207-39Ω	Beyschlag		2	
	Resistor, Carbon Film, 47Ω, ¼W, 5%	R93	SBB0207-47Ω	Beyschlag		1	

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proteon associates, inc.

FSCM NO. 9F914

DRAWN | DATE | USED ON: | DWG. NO. 175-007 | REV. Ø

CHECKED

ISSUED | 3-16-81 | SHEET 3 of 8

PARTS LIST

ASSEMBLY NAME: _____

ASSEMBLY NO.: _____

ASSEMBLY DRWG. NO.: _____

JOB NO. _____

pro88™ Microprocessor Compatible Frequency Synthesizer

[ ] used on C/N 001, 003 only

ITEM NO.	DESCRIPTION	REF. DES.	PART NO./DRWG. NO.	MFGR.	REV.	QTY/ UNIT	QTY/ REQ
	Resistor, Carbon Film, 51Ω, ¼W, 5%	R69	SBB0207-51Ω	Beyschlag		1	
	Resistor, Carbon Film, 68Ω, ¼W, 5%	R57	SBB0207-68Ω	Beyschlag		1	
	Resistor, Carbon Film, 100Ω, ¼W, 5%	R10, 21, 27, 34, 42, 68, 92, 120, 132	SBB0207-100Ω	Beyschlag		9	
	Resistor, Carbon Film, 150Ω, ¼W, 5%	R61, 88, 95, 97	SBB0207-150Ω	Beyschlag		4	
	Resistor, Carbon Film, 220Ω, ¼W, 5%	R83	SBB0207-220Ω	Beyschlag		1	
	Resistor, Carbon Film, 330Ω, ¼W, 5%	R52, 122	SBB0207-330Ω	Beyschlag		2	
	Resistor, Carbon Film, 270Ω, ¼W, 5%	R127, 129	SBB0207-270Ω	Beyschlag		2	
	Resistor, Carbon Film, 470Ω, ¼W, 5%	R11, 22, 23, 47, 50, 51, 89-91, 117-119, 128, 130, 131, 133	SBB0207-470Ω	Beyschlag		16	
[ ]	Resistor, Carbon Film, 1KΩ, ¼W, 5%	R9, 20, 24, 28, 33, 46, 66, 67, 70, 72, 74, 76, 79-82, 112, 121, 123-125, [136-140]	SBB0207-1KΩ	Beyschlag		26	
	Resistor, Carbon Film, 2.2KΩ, ¼W, 5%	R16, 26, 29, 103, 108	SBB0207-2.2KΩ	Beyschlag		5	

PARTS LIST

ASSEMBLY NAME: _____

ASSEMBLY NO.: _____

ASSEMBLY DRWG. NO.: _____

JOB NO. _____

pro88™ Microprocessor Compatible Frequency Synthesizer

ITEM NO.	DESCRIPTION	REF. DES.	PART NO./DRWG. NO.	MFGR.	REV.	QTY/ UNIT	QTY/ REQ
	Resistor, Carbon Film, 2.7KΩ, ¼W, 5%	R12, 84	SBB0207-2.7KΩ	Beyschlag		2	
	Resistor, Carbon Film, 3.3KΩ, ¼W, 5%	R99	SBB0207-3.3KΩ	Beyschlag		1	
	Resistor, Carbon Film, 4.7KΩ, ¼W, 5%	R15, 25, 30, 87, 109	SBB0207-4.7KΩ	Beyschlag		5	
	Resistor, Carbon Film, 6.8KΩ, ¼W, 5%	R13, 85	SBB0207-6.8KΩ	Beyschlag		2	
	Resistor, Carbon Film, 10KΩ, ¼W, 5%	R40, 43, 105, 115, 126	SBB0207-10KΩ	Beyschlag		5	
	Resistor, Carbon Film, 12KΩ, ¼W, 5%	R100	SBB0207-12KΩ	Beyschlag		1	
	Resistor, Carbon Film, 22KΩ, ¼W, 5%	R77, 101	SBB0207-22KΩ	Beyschlag		2	
	Resistor, Carbon Film, 100KΩ, ¼W, 5%	R2, 4, 17, 32, 64, 111	SBB0207-100KΩ	Beyschlag		6	

PARTS LIST

ASSEMBLY NAME: _____

ASSEMBLY NO.: _____

ASSEMBLY DRWG. NO.: _____

JOB NO. _____

pro88™ Microprocessor Compatible Frequency Synthesizer

* Means part not used

ITEM NO.	DESCRIPTION	REF. DES.	PART NO./DRWG. NO.	MFGR.	REV.	QTY/ UNIT	QTY/ REQ
	Resistor, Carbon Film (see Config. Sheet)	R5-8, 11, 18, 19, 35-39, 41, 44, 45, 48, 53-55, 59-62, 73, 75, 78, 94, 96-98, 103, 104, 106, 107, 113, 114, 116	SBB0207-XX	Beyschlag		49	
*	Resistor Pack, Sip Network		764-1-R1K	Beckman		1	
*	Resistor Pack, Sip Network,		783-1-R1K	Beckman		1	
	Resistor,Pot, 100KΩ	R3	72PR100K	Helitrim		1	
	Resistor,Pot, 20KΩ	R63, 102	72PR20K	Helitrim		2	
	Resistor,Pot, 1KΩ	R71	72PR1K	Helitrim		1	
*	Magnitude Comparator		DM8160	National		1	
*	Inverter	U2, 15, 30	74LS04	TI		3	
*	Tri State Buffer		8098	National		1	
*	Parallel Bidirectional Driver		8226	Intel		2	
*	Programmable Peripheral Interface		8255	Intel		1	
*	8-bit Serial/Parallel Register		74LS164	TI		1	

PARTS LIST

ASSEMBLY NAME: _____

ASSEMBLY NO.: _____

ASSEMBLY DRWG. NO.: _____

JOB NO. _____

pro88™ Microprocessor Compatible Frequency Synthesizer

* Means part not used

ITEM NO.	DESCRIPTION	REF. DES.	PART NO./DRWG. NO.	MFGR.	REV.	QTY/ UNIT	QTY/ REQ
*	Quad 2 input AND gate		74LS02	TI		1	
	Dual 4 input NAND gate	U12	74LS20	TI		1	
	Serial input synth chip	U16, 17	145156	Motorola		2	
	(see Config. Sheet)	U18	(see Config. Sheet)	Motorola		1	
	Voltage controlled osc.	U20, 33	1648	Motorola		2	
	Quad 2 input NOR gate	U21, 34	10102	Fairchild		2	
	Triple line receiver	U23, 29	10116	Fairchild		2	
	Phase detector	U24	12040	Fairchild		1	
	(see Config. Sheet)	U27, 28	10136	Fairchild		1	
	Programmable divider	U35	10016	Fairchild		1	
	Quad low power op amp	U22, 31	LM324	National		2	
	Settable positive volt. reg.	U14, 19, 25, 32	LM723	National		4	
	Positive 5v regulator	U13, 26	LM340.T5	National		2	
	Positive 8v regulator	U36	LM340.T8	National		1	
*	Interface (user supplied)						

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FSCM NO. 9F914

DRAWN | DATE | CHECKED | ISSUED

USED ON:

DWG. NO. 175-007 | REV. Ø

3-16-81 | SHEET 7 of 8

PARTS LIST

ASSEMBLY NAME: _____

ASSEMBLY NO.: _____

ASSEMBLY DRWG. NO.: _____

JOB NO. _____

pro88™ Microprocessor Compatible Frequency Synthesizer

* Means part not used

ITEM NO.	DESCRIPTION	REF. DES.	PART NO./DRWG. NO.	MFGR.	REV.	QTY/ UNIT	QTY/ REQ
	Mixer	M1	MD108	Anzac		1	
*	8PST dip switch		76B08	Grayhill		1	
	10MHz crystal	Y1	C130-007	Proteon		1	
	Card ejectors	--	CBE-1	Richco		2	
	Socket, low profile, 14 pin	XU2, 4, 8-12, 14, 15, 19, 20, 22, 24, 25, 30-33	DILB14P-108	Burndy		18	
	Socket, low profile, 16 pin	XU1, 3, 5, 6, 18, 21, 23, 27, 28, 34, 35	DILB16P-108	Burndy		12	
	Socket, low profile, 20 pin	XU16, 17	DILB20P-108	Burndy		2	
	Socket, low profile, 40 pin	XU7	DILB40P-108	Burndy		1	
	SMA right angle PC (see Config. Sheet)	J2-4					

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proteon associates, inc.

FSCM NO.	DRAWN	DATE	USED ON:	DWG. NO.	REV.
9F914	CHECKED			175-007	Ø
	ISSUED			3-16-81	SHEET 8 of8

5. SCHEMATICS

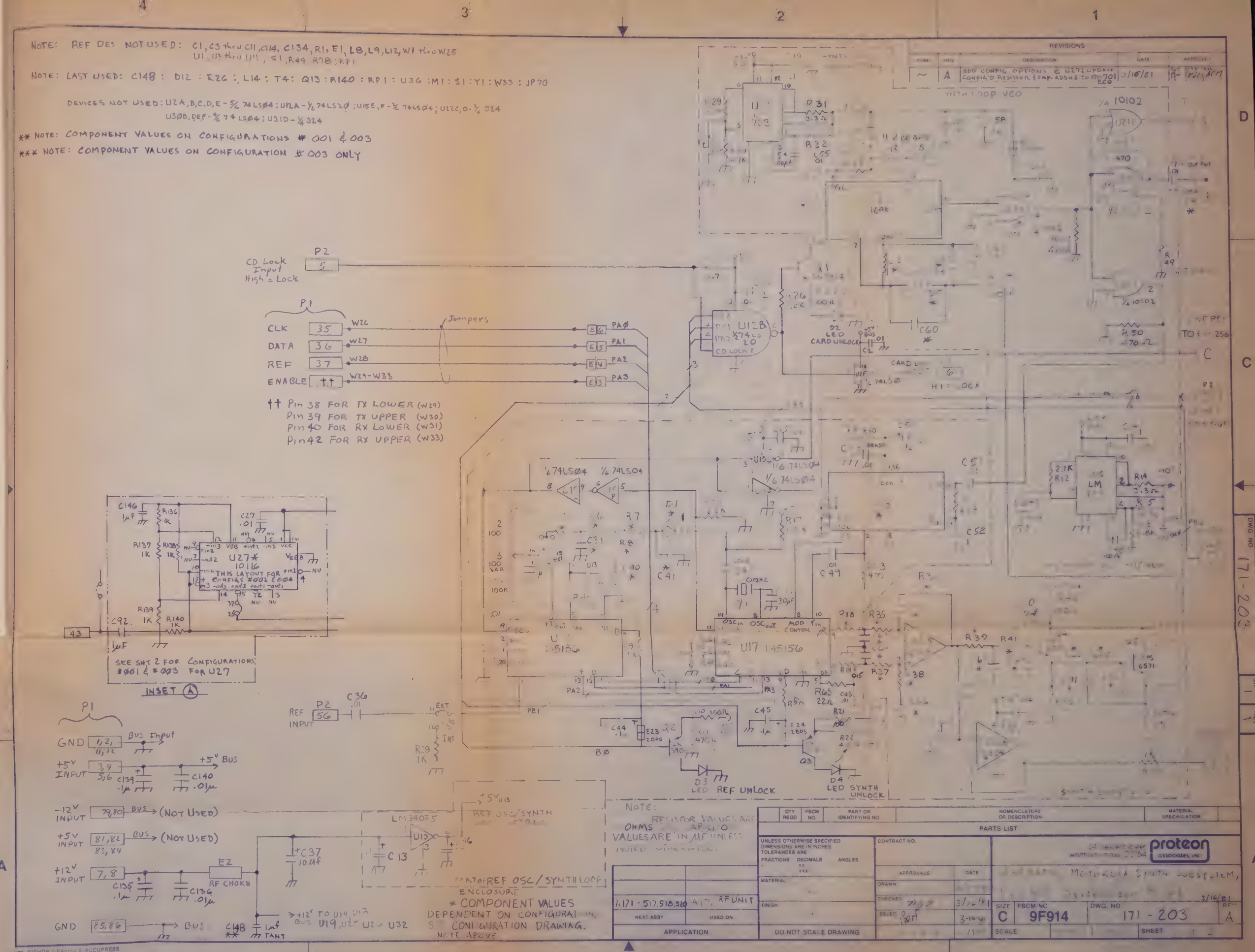
NOTE: REF DES NOT USED: C1, C3 thru C11, C114, C134, R1, E1, L8, L9, L12, W1 thru W25
U1, U3 thru U11, S1, R49 R78; RP1

NOTE: LAST USED: C148 : D12 : E26 : L14 : T4 : Q13 : R140 : RP1 : U36 : M1 : S1 : Y1 : W33 : JP70

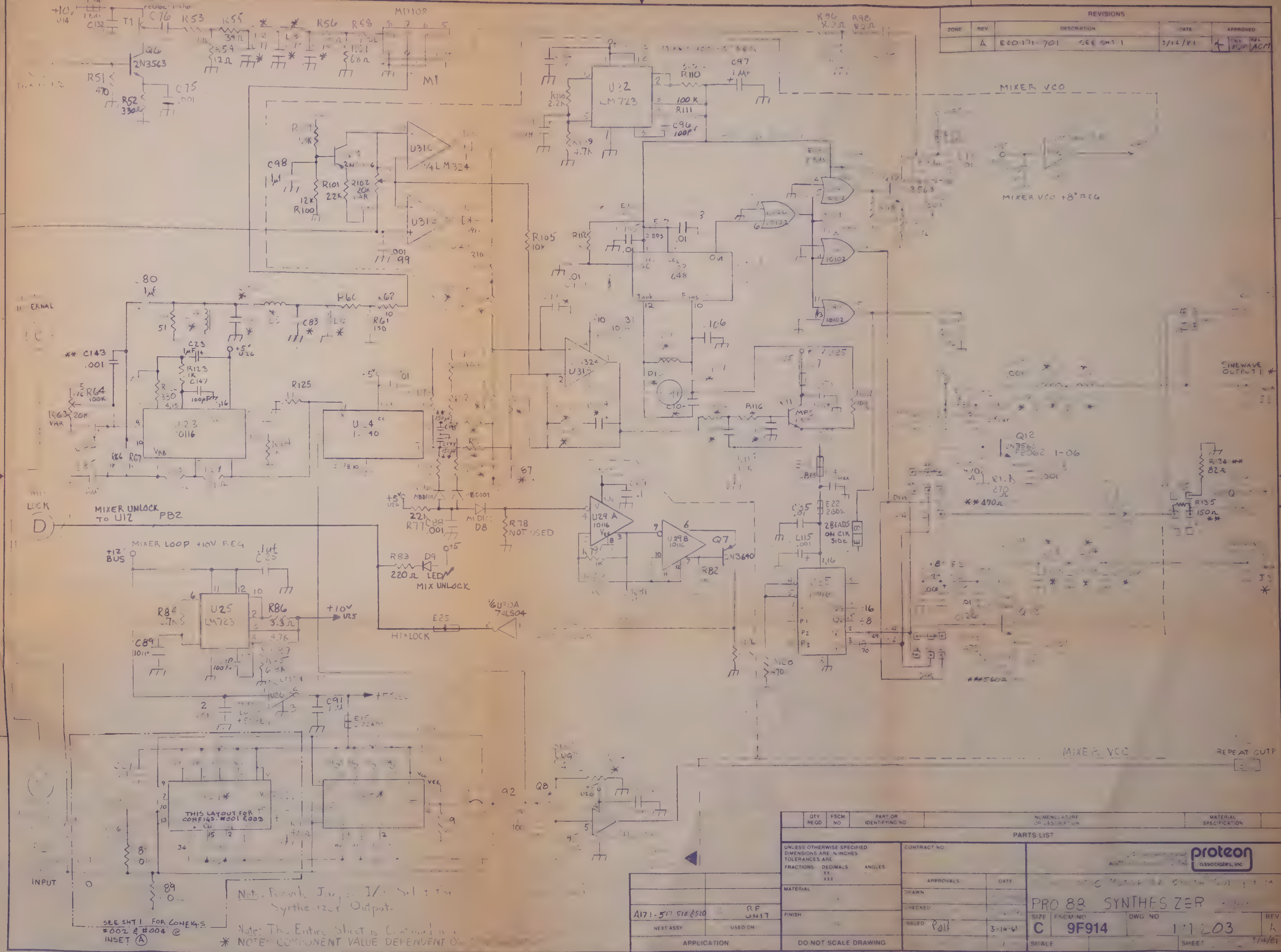
DEVICES NOT USED: U2A,B,C,D,E - 5/6 74LS04; U12A - 1/2 74LS20; U15E,F - 3/6 74LS04; U22C,D - 1/4 324
U30B,DEF - 5/6 74LS04; U31D - 1/4 324

** NOTE: COMPONENT VALUES ON CONFIGURATIONS # 001 & 003

*** NOTE: COMPONENT VALUES ON CONFIGURATION # 003 ONLY



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ECO 171-701 SEE SHT 1	3/16/81	



QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.XX
.XXX

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN	
CHECKED	
ISSUED	3-14-81

A171-517 518 & 520 — RF UNIT
NEXT ASSY — USED ON
APPLICATION

proteon associates, inc

PRO 88 SYNTHESIZER

SIZE C — FSCM NO 9F914 — DWG NO 171203 — REV A

SCALE — SHEET — 3/16/81

DWG NO 171-202 — SH 2 — REV A

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-5972

APPENDIX A

8080 CROSS ASSEMBLER

(This section not used.)

APPENDIX B

USER CONFIGURATION

JOB NO.: A171 APPLICATION: TX UPPER

PRO88 CONFIGURATION CONTROL DOCUMENT

CONFIGURATION NO.: [illegible]

REF PLL

EXT	✓
INT	
FREQ	5 MHz
÷ R	8
÷ N	4
f_Q	1.25 MHz
VCXO: F_0	10 MHz
K_V	785

PLL CONSTANTS

K	3125
N	8
z	.7
Wn	2
K_Q	.4 V/Rad

PLL COMPONENTS

R5	10K
R6	1M
R7	100K
R8	68K
C17	43PF
C39	.01
C40	1µF
C41	.01
D1	MV3102

STEP PLL

XTAL FREQ 10 MHz

÷ R	8
÷ N	91 to 96
f_Q	1.25 MHz
VCO f_0	113.75 to 120 MHz
VCO K_V	2.56×10^7
Prescaler ÷	5/9
Vcune	2.5 to 7.0 volts

PLL CONSTANTS

K	1.02×10^7	K_Q	.4 V/rad
N	96		
z	.5		
Wn	125K		

PLL COMPONENTS

R18	3.3K	R38	6.8K
R19	3.3K	C63	100PF
R35	3.3K	C64	100PF
R36	6.8K	C65	.001 NPO
R37	3.3K	C66	.001 NPO

ACTIVE FILTER

f_c 1.5×10^6 MHz

COMPONENTS

R39	—	C68	—
R41	—	C69	—
R44	6.8K	C71	150PF
R45	6.8K	C72	47PF

VCO COMPONENTS

L1	56 #26 AWG T30-0	R34	100
D5	MV3102	C61	1000PF (NPO)
C60*	8 PF		
U18	12011		

REPEAT PLL

INPUT L.P.F.(M1) f_c 120 Type cheb 1dB

L2	62nH	C78	47pF
L3	62nH	C79	30PF
C77	30pF		

OUTPUT FILTER (M1)

FREQ 4 - 5.25 MHz

B.P. _____ L.P. ✓

L4	—	C81	1000PF NPO
L5	1µH	C82	short
L6	—	C83	1000PF NPO

REPEAT INPUT

EXT ✓ INT _____

FREQ 64-84 MHz

÷ N 16 U27, U28

RPT F_0 4 - 5.25 MHz

VCO

F_0 119 to 125 MHz

K_V 2.56×10^7 Rad/volt sec

Vcune 2.5 to 7.0 volts

PLL CONSTANTS

K 3×10^6 sec K_Q = .12

N 1 z .7

Wn 5×10^4

PLL COMPONENTS

R73	330	R116	6.8K	C104	.1 cer
R75	330	R132	100	C107	.001
R104	15K	C86	150PF cer	C108	8pF
R106	68K	C87	150PF cer	C109	150PF
R107	68K	C100	.1 cer	C110	22PF
R113	15K	C102	—	D10	MV3102
R114	6.8K	C103	—	L7	56 #26 AWG T30-0

REPEAT PLL (Cont'd.)

OUTPUT Monitor f_0 = 59.5 - 62.5 MHz

Sinewave #1 f_0 = 59.5 - 62.5 MHz Type cheb 1dB

f_c	62.5	L10	.139	L11	.139
C120	100	C121	150	C122	100

Sinewave #2 f_0 = 29.75 - 31.25 MHz Type cheb 1dB

f_c	35 MHz	L13	248nH	L14	248nH
C128	200	C129	270	C130	200

f_0 #1 59.5 - 62.5 f_0 #2 29.75 - 31.25

P_0 #1 +3dbm P_0 #2 +3dbm

JUMPERS

REF PLL

EXT 10-11	✓
13-15	✓
INT 10-12	
13-14	
U16, ÷ R	8
16-17	✓
16-18	✓
16-19	✓

STEP PLL

÷ R	8
20-21	✓
20-22	✓
20-23	✓

REPEAT PLL

÷ N	16
26-27	
26-28	
26-29	
26-30	
26-31	
26-32	
26-33	
26-34	
26-45	

REPEAT PLL (cont)

35-36	
35-37	
35-38	
35-39	✓
35-40	
35-41	
35-42	
35-43	
44-45	
44-46	✓
44-47	

OUTPUTS

FREQ 1 P2-50

58-59	
58-60	
66-67	

BUFFER 1 INPUT

48-49	✓
48-50	
48-51	

FREQ 2 P2-38 (Monitor) -11dbm ECL

61-68	✓
61-62	
61-63	
48-52	✓

OUTPUTS (cont)

BUFFER 2 INPUT

53-54	✓
53-55	
53-56	
DELAY	NA
1-2	
1-3	
1-4	
1-5	
1-6	
1-7	
1-8	
1-9	
1-10	
ADDRESS	NA

UNUSED

Q8

J4 on units 2→5

* Refer to section 4 i

PCB NO.: A171 APPLICATION: TX LOWER

PROGRAM CONFIGURATION CONTROL DOCUMENT

REF PLL

EXT	✓
INT	
FREQ	5 MHz
÷ R	8
÷ N	4
f_Q	1.25 MHz
VCXO: F_0	10 MHz
K_V	285

PLL CONSTANTS

K	312.5
N	8
z	.7
Wn	2
K_Q	.4 v/rad

PLL COMPONENTS

R5	10K
R6	1M
R7	100K
R8	68K
C17	43 PF
C39	.01
C40	1 µF tant
C41	.01
D1	MV3102

STEP PLL

XTAL FREQ 10 MHz

÷ R	64
÷ N	810 to 1066
f_Q	.15625 MHz
VCO f_0	127 to 167 MHz
VCO K_V	
Prescaler ÷	10/11
V_{tune}	2.5 to 7.0 volts

PLL CONSTANTS

K	1.5×10^7	K_Q =	
N	1066		
z	.7		
Wn	20K		

PLL COMPONENTS

R18	6.8K	R38	12K
R19	6.8K	C63	100 PF
R35	6.8K	C64	100 PF
R36	12K	C65	.01
R37	6.8K	C66	.01

ACTIVE FILTER

f_c 67 KHz

COMPONENTS

R39	—	C68	—
R41	—	C69	—
R44	18K	C71	390 PF (WPO)
R45	18K	C72	100 PF (WPO)

VCO COMPONENTS

L1	56 # 26 awg T25-8	R34	100
D5	MV3102	C61	.001
C60	—		

REPEAT PLL

INPUT L.P.F. (M1) f_c 170 MHz Type cheb 1dB

L2	51nH	C78	56 PF
L3	51nH	C79	39 PF
C77	39PF		

OUTPUT FILTER (M1)

FREQ 1.15 - 2.05 MHz

B.P. _____ L.P. ✓

L4	—	C81	1000 PF (WPO)
L5	1 µH	C82	short
L6	—	C83	1000 PF (WPO)

U18 MC 12013

REPEAT INPUT

EXT ✓ INT _____

FREQ 1.6 MHz ± .45H

÷ N 1 U27, U28

RPT F_0 1.15 - 2.05 MHz

VCO

F_0 128 to 168 MHz

K_V _____

V_{tune} 2.5 - 7.0 volts

PLL CONSTANTS

K	4.5×10^6	K_Q =	
N	1	z	.7
Wn	20K		

PLL COMPONENTS

R73	3.3K	R116	1.2K	C104	.1 µF
R75	3.3K	R132	100	C107	.001
R104	680	C86	100 PF	C108	—
R106	100K	C87	100 PF	C109	.01 cer
R107	100K	C100	.1 µF	C110	—
R113	680	C102	—	D10	MV3102
R114	1.2K	C103	—	L7	56 # 26 awg T25-8

REPEAT PLL (Cont'd.)

OUTPUT

Sinewave #1 f_0 = _____ Type _____ NONE

f_c	L10	L11
C120	C121	C122

Sinewave #2 f_0 = _____ Type None

f_c	L13	L14
C128	C129	C130

f_0 #1 _____ f_0 #2 _____

JUMPERS

REF PLL

EXT 10-11	✓
13-15	✓
INT 10-12	
13-14	
U16, ÷ R	8
16-17	✓
16-18	✓
16-19	✓

STEP PLL

÷ R	64
20-21	✓
20-22	✓
20-23	

REPEAT PLL

÷ N	1
26-27	
26-28	
26-29	
26-30	
26-31	
26-32	
26-33	
26-34	
26-45	

REPEAT PLL (cont)

35-36	
35-37	
35-38	
35-39	
35-40	
35-41	
35-42	
35-43	
44-45	
44-46	
44-47	
46-47	✓

OUTPUTS

FREQ 1 P2-50 ECL output AC

58-59	✓
58-60	
66-67	

BUFFER 1 INPUT

48-49	
48-50	✓
48-51	

FREQ 2 P2-38 NU

61-68	
61-62	
61-63	
48-52	✓

OUTPUTS (cont)

BUFFER 2 INPUT NU

53-54	
53-55	
53-56	
DELAY	NU
1-2	
1-3	
1-4	
1-5	
1-6	
1-7	
1-8	
1-9	
1-10	
ADDRESS	NU

UNUSED

Q8

J2

J3 on units 2-5

* Refer to Section 4

JOB NO.: 4171 APPLICATION: R X UPPER

PR088 CONFIGURATION CONTROL DOCUMENT

CONFIGURATION NO.: 003

REF PLL

EXT	✓
INT	
FREQ	5 MHz
÷ R	8
÷ N	4
f_Q	1.25 MHz
VCXO: F_0	10 MHz
K_V	785

PLL CONSTANTS

K	312.5
N	8
z	.7
Wn	7
K_Q	.4 v/Rad

PLL COMPONENTS

R5	10K
R6	1M
R7	100K
R8	68K
C17	43 PF
C39	.01
C40	1 µF
C41	.01
D1	MV3102

STEP PLL

XTAL FREQ 10 MHz

÷ R	8
÷ N	40 to 51
f_Q	1.25 MHz
VCO f_0	50 to 63.75 MHz
VCO K_V	187×10^6
Prescaler ÷	5/6
Vcune	2.5 - 20 Volts

PLL CONSTANTS

K	7.48×10^6
K_Q	.4
N	51
z	.5
Wn	10K

PLL COMPONENTS

R18	3.9K	R38	8.2K
R19	3.9K	C63	100PF
R35	4.7K	C64	100 PF
R36	8.2K	C65	.001
R37	4.7K	C66	.001

ACTIVE FILTER

f_c 2.2×10^6 MHz

COMPONENTS

R39	—	C68	—
R41	—	C69	—
R44	6.8K	C71	120PF
R45	6.8K	C72	33 PF

VCO COMPONENTS

L1	T30-8 16C #30 enm	R34	100
D5	MV3102	C61	220PF (NPO)
C60	8 PF		

U18 MC12009

Omit Q4

REPEAT PLL

INPUT L.P.F.(M1) f_c 62.5 Type Cheb 1dB

L2	.139 µH	C78	150
L3	.139 µH	C79	100
C77	100		

OUTPUT FILTER (M1)

FREQ 5.625 - 6.875 MHz

B.P. _____ L.P. ✓

L4	—	C81	1000 NPO
L5	1 µH	C82	short
L6	—	C83	1000 NPO

REPEAT INPUT

EXT _____ INT ✓

FREQ 45 - 55 MHz

÷ N 8 U27, U28

RPT F_0 5.625 - 6.875 MHz

VCO

F_0 56 to 70

K_V 2.86×10^7

Vcune 2.5 - 20 Volts

PLL CONSTANTS

K 3.42×10^6 K_Q =

N 1 z .5

Wn 150K

PLL COMPONENTS

R73	4.7K	R116	6.8K	C104	.01 cer
R75	4.7K	R132	100	C107	.001
R104	1.5K	C86	100 PF	C108	—
R106	4.7K	C87	100 PF	C109	100PF
R107	4.7K	C100	.01 cer	C110	33 PF
R113	1.5K	C102	—	D10	MV3102
R114	6.8K	C103	—	L7	T30-8 16C #30 enm

REPEAT PLL (Cont'd.)

OUTPUT

Sinewave #1 f_0 = 28-35 MHz Type Cheb 1dB

f_c	35 MHz	L10	248 nH	L11	248 nH
C120	200 PF	C121	270 PF	C122	200 PF

Sinewave #2 f_0 = _____ Type None

f_c		L13		L14	
C128		C129		C130	

f_0 #1 28-35 MHz f_0 #2 _____

P_0 #1 +3dbm

JUMPERS

REF PLL		REPEAT PLL (cont)		OUTPUTS (cont)	
EXT 10-11	✓	35-36		BUFFER 2 INPUT	
13-15	✓	35-37		53-54	
INT 10-12		35-38	✓	53-55	
13-14		35-39		53-56	✓ TEST
U16, ÷ R	8	35-40		DELAY	NU
16-17	✓	35-41		1-2	
16-18	✓	35-42		1-3	
16-19	✓	35-43		1-4	
STEP PLL		44-45		1-5	
÷ R	8	44-46	✓	1-6	
20-21	✓	44-47		1-7	
20-22	✓			1-8	
20-23	✓	**OUTPUTS**		1-9	
REPEAT PLL		FREQ 1 P2-50		1-10	
÷ N	8	58-59		ADDRESS	NU
26-27		58-60			
26-28		66-67			
26-29		BUFFER 1 INPUT			
26-30		48-49			
26-31		48-50	✓		
26-32		48-51			
26-33		FREQ 2 P2-38 (Monitor output) -11dbm ECL			
26-34		61-68	✓		
26-45	✓ on Back of Board	61-62			
		61-63			
		48-52	✓		

UNUSED

U35

L13, L14

C128, 129, 13

Q8

J3, 4 on units 2-5

* Refer to section 4

JOB NO.: 1171 APPLICATION: RX LOWER

PROBE CONFIGURATION CONTROL DOCUMENT

REF PLL

EXT	✓
INT	
FREQ	5 MHz
÷ R	8
÷ N	4
f_Q	1.25 MHz
VCXO: F_o	10 MHz
K_v	705

PLL CONSTANTS

K	312.5
N	8
z	.7
Wn	2
K_Q	.4 v/rad

PLL COMPONENTS

R5	10K
R6	1M
R7	100K
R8	68K
C17	43 PF
C39	.01 µf
C40	1 µF
C41	.01 µF
D1	MV3102

STEP PLL

XTAL FREQ 10 MHz

÷ R	64
÷ N	569 to 700
f_Q	0.15625 MHz
VCO f_o	89 to 110 MHz
VCO K_v	2.56×10^7
Prescaler ÷	8/9
Vcune	2.5 to 20 volts

PLL CONSTANTS

K	1.02×10^7	K_Q	.4
N	701		
z	.7		
Wn	20K		

PLL COMPONENTS

R18	1.8K	R38	6.8K
R19	1.8K	C63	100 PF
R35	1.8K	C64	100 PF
R36	6.8K	C65	.01
R37	1.8K	C66	.01

ACTIVE FILTER

f_c 33 KHz

COMPONENTS

R39	none	C68	none
R41	none	C69	none
R44	10K	C71	330 PF (NPO)
R45	10K	C72	270 PF (NPO)

VCO COMPONENTS

L1	CE #26 4 cy T30-0	R34	100
D5	MV3102	C61	.001
C60	2 PF	Q8	none
U18	MC12011P		

REPEAT PLL

INPUT L.P.F. (M1) f_c 110 MHz Type LPF Cheb 1dB

L2	79 µH	C78	87 PF
L3	79 µH	C79	62 PF
C77	62 PF		

OUTPUT FILTER (M1)

FREQ 88 kHz – 1.12 MHz

B.P. _____ L.P. ✓

L4	0	C81	.001 NPO
L5	1 mH	C82	0
L6	0	C83	.001 NPO
U27	10116	U28	none

REPEAT INPUT

EXT _____ INT ✓

FREQ 600 ± 512 kHz

÷ N 1 U27, U28

RPT F_o 88 kHz – 1.12 MHz

VCO

F_o 90 MHz to 110 MHz

K_v 3.142×10^7

Vcune 2.5 to 20 volts

PLL CONSTANTS

K	3.77×10^6	K_Q	.12
N	1	z	.7
Wn	20K		

PLL COMPONENTS

R73	39K	R116	10K	C104	.1
R75	39K	R132	100	C107	.001
R104	680	C86	100 PF	C108	0
R106	39K	C87	100 PF	C109	.001 µ NPO
R107	39K	C100	.1	C110	270 PF
R113	680	C102	—	D10	MV3102
R114	10K	C103	—	L7	CE #26 T30-0

REPEAT PLL (Cont'd.)

OUTPUT

Sinewave #1 f_o = _____ Type None

f_c		L10		L11	
C120		C121		C122	

Sinewave #2 f_o = _____ Type None

f_c		L13		L14	
C128		C129		C130	

f_o #1 _____ f_o #2 _____

JUMPERS

REF PLL		REPEAT PLL (cont)		OUTPUTS (cont)	
EXT 10-11	✓	35-36		BUFFER 2 INPUT	NU
13-15	✓	35-37	✓	53-54	
INT 10-12		35-38		53-55	
13-14		35-39		53-56	✓ TEST
U16, ÷ R	8	35-40		DELAY	NA
16-17	✓	35-41		1-2	
16-18	✓	35-42		1-3	
16-19	✓	35-43		1-4	
STEP PLL		44-45		1-5	
÷ R	64	44-46	✓	1-6	
20-21	✓	44-47		1-7	
20-22	✓			1-8	
20-23		**OUTPUTS**		1-9	
REPEAT PLL		FREQ 1 P2-50	ECL OUTPUT AC	1-10	
÷ N	1	58-59	✓	ADDRESS	
26-27		58-60			NA
26-28		66-67			
26-29		BUFFER 1 INPUT			
26-30		48-49			
26-31		48-50			
26-32		48-51	✓		
26-33		FREQ 2 P2-38	NU		
26-34		61-68			
26-45		61-62			
		61-63			
		48-52	✓		

UNUSED

U27, 28

J2

J3 on units 2→5

Q8

* Refer to section 4

STDN LIBRARY

NO. ME-7942

TITLE: PRO88 FREQUENCY SYNTHESIZER

C.2

NAME/PHONE/ORGANIZATION	DATE

MP MASTER
MA33918